

FEATURES

- Accurate rms-to-dc conversion from 50 Hz to 6 GHz
- Single-ended input dynamic range of >50 dB
- No balun or external input tuning required
- Waveform and modulation independent, such as
GSM/CDMA/W-CDMA/TD-SCDMA/WiMAX/LTE
- Linear-in-decibels output, scaled: 52 mV/dB
- Log conformance error: $<\pm 0.15$ dB
- Temperature stability: $<\pm 0.5$ dB
- Voltage supply range: 4.5 V to 5.5 V
- Operating temperature range: -40°C to $+125^{\circ}\text{C}$
- Power-down capability to 1.5 mW
- Small footprint, 4 mm \times 4 mm, LFCSP

APPLICATIONS

- Power amplifier linearization/control loops
- Transmitter power controls
- Transmitter signal strength indication (TSSI)
- RF instrumentation

GENERAL DESCRIPTION

The AD8363 is a true rms responding power detector that can be directly driven with a single-ended 50 Ω source. This feature makes the AD8363 frequency versatile by eliminating the need for a balun or any other form of external input tuning for operation up to 6 GHz.

The AD8363 provides an accurate power measurement, independent of waveform, for a variety of high frequency communication and instrumentation systems. Requiring only a single supply of 5 V and a few capacitors, it is easy to use and provides high measurement accuracy. The AD8363 can operate from arbitrarily low frequencies to 6 GHz and can accept inputs that have rms values from less than -50 dBm to at least 0 dBm, with large crest factors exceeding the requirements for accurate measurement of WiMAX, CDMA, W-CDMA, TD-SCDMA, multicarrier GSM, and LTE signals.

The AD8363 can determine the true power of a high frequency signal having a complex low frequency modulation envelope, or it can be used as a simple low frequency rms voltmeter. The high-pass corner generated by its internal offset-nulling loop can be lowered by a capacitor added on the CHPF pin.

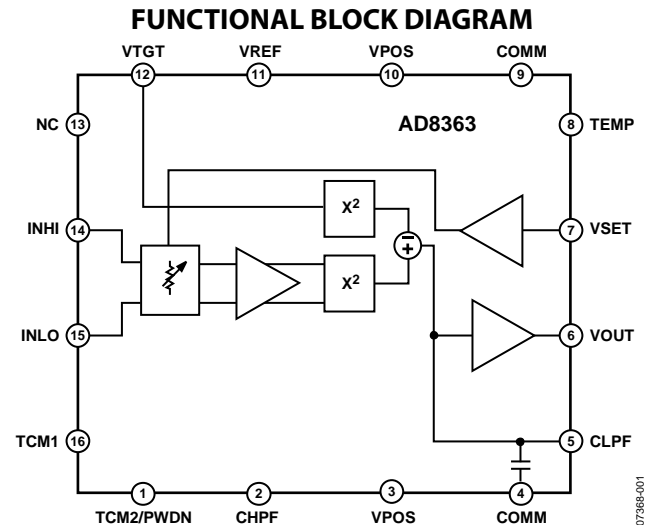


Figure 1.

Used as a power measurement device, VOUT is connected to VSET. The output is then proportional to the logarithm of the rms value of the input. The reading is presented directly in decibels and is conveniently scaled to 52 mV/dB, or approximately 1 V per decade; however, other slopes are easily arranged. In controller mode, the voltage applied to VSET determines the power level required at the input to null the deviation from the setpoint. The output buffer can provide high load currents.

The AD8363 has 1.5 mW power consumption when powered down by a logic high applied to the TCM2/PWDN pin. It powers up within about 30 μs to its nominal operating current of 60 mA at 25°C. The AD8363 is available in a 4 mm \times 4 mm 16-lead LFCSP for operation over the -40°C to $+125^{\circ}\text{C}$ temperature range.

A fully populated RoHS-compliant evaluation board is also available.

Rev. 0

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REVISION HISTORY

5/09—Revision 0: Initial Version

SPECIFICATIONS

$V_{POS} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $Z_O = 50\ \Omega$, single-ended input drive, V_{OUT} connected to V_{SET} , $V_{TGT} = 1.4\text{ V}$, $C_{LPF} = 3.9\text{ nF}$, $C_{HPF} = 2.7\text{ nF}$, error referred to best-fit line (linear regression) from -20 dBm to -40 dBm , unless otherwise noted. Negative current values imply that the AD8363 is sourcing current out of the indicated pin.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Maximum Input Frequency				6	GHz
RF INPUT INTERFACE					
Input Resistance	INHI (Pin 14), INLO (Pin 15), ac-coupled Single-ended drive		50		Ω
Common-Mode DC Voltage			2.6		V
100 MHz					
Output Voltage: High Power In	TCM1 (Pin 16) = 0.47 V, TCM2 (Pin 1) = 1.0 V, INHI input $P_{IN} = -10\text{ dBm}$		2.47		V
Output Voltage: Low Power In	$P_{IN} = -40\text{ dBm}$		0.92		V
$\pm 1.0\text{ dB}$ Dynamic Range	CW input, $T_A = 25^\circ\text{C}$		65		dB
Maximum Input Level, $\pm 1.0\text{ dB}$			9		dBm
Minimum Input Level, $\pm 1.0\text{ dB}$			-56		dBm
Deviation vs. Temperature	Deviation from output at 25°C $-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -10\text{ dBm}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -40\text{ dBm}$		-0.2/+0.3 -0.5/+0.6		dB
Logarithmic Slope			51.7		mV/dB
Logarithmic Intercept			-58		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 40 dB dynamic range 12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range 14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		< ± 0.1 < ± 0.1 < ± 0.1		dB
	256 QAM, CF = 8 dB, over 40 dB dynamic range		< ± 0.1		dB
Input Impedance	Single-ended drive		49 - j0.09		Ω
900 MHz					
Output Voltage: High Power In	TCM1 (Pin 16) = 0.5 V, TCM2 (Pin 1) = 1.2 V, INHI input $P_{IN} = -15\text{ dBm}$		2.2		V
Output Voltage: Low Power In	$P_{IN} = -40\text{ dBm}$		0.91		V
$\pm 1.0\text{ dB}$ Dynamic Range	CW input, $T_A = 25^\circ\text{C}$		54		dB
Maximum Input Level, $\pm 1.0\text{ dB}$			-2		dBm
Minimum Input Level, $\pm 1.0\text{ dB}$			-56		dBm
Deviation vs. Temperature	Deviation from output at 25°C $-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -15\text{ dBm}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -40\text{ dBm}$		+0.6/-0.4 +0.8/-0.6		dB
Logarithmic Slope			51.8		mV/dB
Logarithmic Intercept			-58		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 40 dB dynamic range 12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range 14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		< ± 0.1 < ± 0.1 < ± 0.1		dB
	256 QAM, CF = 8 dB, over 40 dB dynamic range		< ± 0.1		dB
Input Impedance	Single-ended drive		60 - j3.3		Ω

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Parameter	Conditions	Min	Typ	Max	Unit
1.9 GHz	TCM1 (Pin 16) = 0.52 V, TCM2 (Pin 1) = 0.51 V, INHI input				
Output Voltage: High Power In	$P_{IN} = -15$ dBm		2.10		V
Output Voltage: Low Power In	$P_{IN} = -40$ dBm		0.8		V
± 1.0 dB Dynamic Range	CW input, $T_A = 25^\circ\text{C}$		48		dB
Maximum Input Level, ± 1.0 dB			-6		dBm
Minimum Input Level, ± 1.0 dB			-54		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -15$ dBm		+0.3/-0.5		dB
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -40$ dBm		+0.4/-0.4		dB
Logarithmic Slope			52		mV/dB
Logarithmic Intercept			-55		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 37 dB dynamic range		± 0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 37 dB dynamic range		± 0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 37 dB dynamic range		± 0.1		dB
	256 QAM, CF = 8 dB, over 37 dB dynamic range		± 0.1		dB
Input Impedance	Single-ended drive		118 - j26		Ω
2.14 GHz	TCM1 (Pin 16) = 0.52 V, TCM2 (Pin 1) = 0.6 V, INHI input				
Output Voltage: High Power In	$P_{IN} = -15$ dBm		2.0		V
Output Voltage: Low Power In	$P_{IN} = -40$ dBm		0.71		V
± 1.0 dB Dynamic Range	CW input, $T_A = 25^\circ\text{C}$		44		dB
Maximum Input Level, ± 1.0 dB			-8		dBm
Minimum Input Level, ± 1.0 dB			-52		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -15$ dBm		+0.1/-0.2		dB
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -40$ dBm		+0.3/-0.5		dB
Logarithmic Slope			52.2		mV/dB
Logarithmic Intercept			-54		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 35 dB dynamic range		± 0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 35 dB dynamic range		± 0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 35 dB dynamic range		± 0.1		dB
	256 QAM, CF = 8 dB, over 35 dB dynamic range		± 0.1		dB
Rise Time	Transition from no input to 1 dB settling at $R_{FIN} = -10$ dBm, $C_{LPF} = 390$ pF, $C_{HPF} = \text{open}$		3		μs
Fall Time	Transition from -10 dBm to within 1 dB of final value (that is, no input level), $C_{LPF} = 390$ pF, $C_{HPF} = \text{open}$		15		μs
Input Impedance	Single-ended drive		130 - j49		Ω
2.6 GHz	TCM1 (Pin 16) = 0.54 V, TCM2 (Pin 1) = 1.1 V, INHI input				
Output Voltage: High Power In	$P_{IN} = -15$ dBm		1.84		V
Output Voltage: Low Power In	$P_{IN} = -40$ dBm		0.50		V
± 1.0 dB Dynamic Range	CW input, $T_A = 25^\circ\text{C}$		41		dB
Maximum Input Level, ± 1.0 dB			-7		dBm
Minimum Input Level, ± 1.0 dB			-48		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -15$ dBm		+0.5/-0.2		dB
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$; $P_{IN} = -40$ dBm		+0.6/-0.2		dB
Logarithmic Slope			52.9		mV/dB
Logarithmic Intercept			-49		dBm

Parameter	Conditions	Min	Typ	Max	Unit
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 32 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 32 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 32 dB dynamic range		±0.1		dB
Input Impedance	256 QAM, CF = 8 dB, over 32 dB dynamic range		±0.1		dB
	Single-ended drive		95 – j65		Ω
3.8 GHz	TCM1 (Pin 16) = 0.56 V, TCM2 (Pin 1) = 1.0 V, INLO input				
Output Voltage: High Power In	P _{IN} = –20 dBm		1.54		V
Output Voltage: Low Power In	P _{IN} = –40 dBm		0.54		V
±1.0 dB Dynamic Range	CW input, T _A = 25°C		43		dB
Maximum Input Level, ±1.0 dB			–5		dBm
Minimum Input Level, ±1.0 dB			–48		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	–40°C < T _A < +85°C; P _{IN} = –20 dBm		+0.1/–0.7		dB
	–40°C < T _A < +85°C; P _{IN} = –40 dBm		+0.4/–0.5		dB
Logarithmic Slope			50.0		mV/dB
Logarithmic Intercept			–51		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 32 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 32 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 32 dB dynamic range		±0.1		dB
Input Impedance	256 QAM, CF = 8 dB, over 32 dB dynamic range		±0.1		dB
	Single-ended drive		42 – j4.5		Ω
5.8 GHz	TCM1 (Pin 16) = 0.88 V, TCM2 (Pin 1) = 1.0 V, INLO input				
Output Voltage: High Power In	P _{IN} = –20 dBm		1.38		V
Output Voltage: Low Power In	P _{IN} = –40 dBm		0.36		V
±1.0 dB Dynamic Range	CW input, T _A = 25°C		45		dB
Maximum Input Level, ±1.0 dB			–3		dBm
Minimum Input Level, ±1.0 dB			–48		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	–40°C < T _A < +85°C; P _{IN} = –20 dBm		+0.1/–0.6		dB
	–40°C < T _A < +85°C; P _{IN} = –40 dBm		+0.3/–0.8		dB
Logarithmic Slope			51.1		mV/dB
Logarithmic Intercept			–47		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (W-CDMA), over 32 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 32 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 32 dB dynamic range		±0.1		dB
Input Impedance	256 QAM, CF = 8 dB, over 32 dB dynamic range		±0.1		dB
	Single-ended drive		28 + j1.6		Ω
OUTPUT INTERFACE	VOUT (Pin 6)				
Output Swing, Controller Mode	Swing range minimum, R _L ≥ 500 Ω to ground		0.03		V
	Swing range maximum, R _L ≥ 500 Ω to ground		4.8		V
Current Source/Sink Capability	Output held at V _{POS} /2			10/10	mA
Voltage Regulation	I _{LOAD} = 8 mA, source/sink		–0.2/+0.1		%
Rise Time	Transition from no input to 1 dB settling at R _{FIN} = –10 dBm, C _{LPF} = 390 pF, C _{HFPF} = open		3		μs
Fall Time	Transition from –10 dBm to within 1 dB of final value (that is, no input level), C _{LPF} = 390 pF, C _{HFPF} = open		15		μs
Noise Spectral Density	Measured at 100 kHz		45		nV/√Hz

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Parameter	Conditions	Min	Typ	Max	Unit
SETPOINT INPUT	VSET (Pin 7)				
Voltage Range	Log conformance error ≤ 1 dB, minimum 2.14 GHz Log conformance error ≤ 1 dB, maximum 2.14 GHz		2.0 0.7		V V
Input Resistance			72		k Ω
Logarithmic Scale Factor	$f = 2.14$ GHz, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		19.2		dB/V
Logarithmic Intercept	$f = 2.14$ GHz, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, referred to 50 Ω		-54		dBm
TEMPERATURE COMPENSATION	TCM1 (Pin 16), TCM2 (Pin 1)				
Input Voltage Range		0		2.5	V
Input Bias Current, TCM1	$V_{\text{TCM1}} = 0$ V $V_{\text{TCM1}} = 0.5$ V		-140 80		μ A μ A
Input Resistance, TCM1	$V_{\text{TCM1}} > 0.7$ V		5		k Ω
Input Current, TCM2	$V_{\text{TCM2}} = 5$ V $V_{\text{TCM2}} = 4.5$ V $V_{\text{TCM2}} = 1$ V $V_{\text{TCM2}} = 0$ V		2 750 -2 -3		μ A μ A μ A μ A
Input Resistance, TCM2	0.7 V $\leq V_{\text{TCM2}} \leq 4.0$ V		500		k Ω
VOLTAGE REFERENCE	VREF (Pin 11)				
Output Voltage	$\text{RF}_{\text{IN}} = -55$ dBm		2.3		V
Temperature Sensitivity	$25^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $70^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq +25^{\circ}\text{C}$		0.04 -0.06 -0.18		mV/ $^{\circ}\text{C}$ mV/ $^{\circ}\text{C}$ mV/ $^{\circ}\text{C}$
Current Source/Sink Capability	$25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A < +25^{\circ}\text{C}$			4/0.05 3/0.05	mA mA
Voltage Regulation	$T_A = 25^{\circ}\text{C}$, $I_{\text{LOAD}} = 3$ mA		-0.6		%
TEMPERATURE REFERENCE	TEMP (Pin 8)				
Output Voltage	$T_A = 25^{\circ}\text{C}$, $R_L \geq 10$ k Ω		1.4		V
Temperature Coefficient	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $R_L \geq 10$ k Ω		5		mV/ $^{\circ}\text{C}$
Current Source/Sink Capability	$25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A < +25^{\circ}\text{C}$			4/0.05 3/0.05	mA mA
Voltage Regulation	$T_A = 25^{\circ}\text{C}$, $I_{\text{LOAD}} = 3$ mA		-0.1		%
RMS TARGET INTERFACE	VTGT (Pin 12)				
Input Voltage Range		1.4		2.5	V
Input Bias Current	$V_{\text{TGT}} = 1.4$ V		14		μ A
Input Resistance			100		k Ω
POWER-DOWN INTERFACE	TCM2 (Pin1)				
Logic Level to Enable	VPWDN decreasing		4.2		V
Logic Level to Disable	VPWDN increasing		4.7		V
Input Current	$V_{\text{TCM2}} = 5$ V $V_{\text{TCM2}} = 4.5$ V $V_{\text{TCM2}} = 1$ V $V_{\text{TCM2}} = 0$ V		2 750 -2 -3		μ A μ A μ A μ A
Enable Time	TCM2 low to V_{OUT} at 1 dB of final value, $C_{\text{LPF}} = 470$ pF, $C_{\text{HPF}} = 220$ pF, $\text{RF}_{\text{IN}} = 0$ dBm		35		μ s
Disable Time	TCM2 high to V_{OUT} at 1 dB of final value, $C_{\text{LPF}} = 470$ pF, $C_{\text{HPF}} = 220$ pF, $\text{RF}_{\text{IN}} = 0$ dBm		25		μ s
POWER SUPPLY INTERFACE	VPOS (Pin 3, Pin 10)				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	$T_A = 25^{\circ}\text{C}$, $\text{RF}_{\text{IN}} = -55$ dBm $T_A = 85^{\circ}\text{C}$		60 72		mA mA
Power-Down Current	$V_{\text{TCM2}} > V_{\text{POS}} - 0.3$ V		300		μ A

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
Input Average RF Power ¹	21 dBm
Equivalent Voltage, Sine Wave Input	2.51 V rms
Internal Power Dissipation	450 mW
θ_{JC}^2	10.6°C/W
θ_{JB}^2	35.3°C/W
θ_{JA}^2	57.2°C/W
Ψ_{JT}^2	1.0°C/W
Ψ_{JB}^2	34°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ This is for long durations. Excursions above this level, with durations much less than 1 second, are possible without damage.

² No airflow with the exposed pad soldered to a 4-layer JEDEC board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

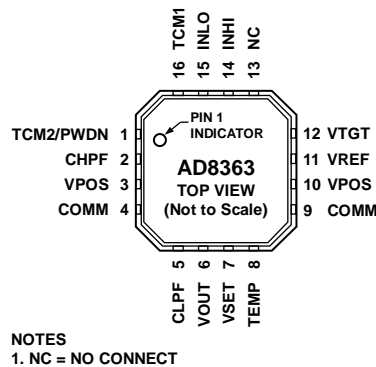


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equivalent Circuit
1	TCM2/PWDN	This is a dual function pin used for controlling the amount of nonlinear intercept temperature compensation at voltages <2.5 V and/or for shutting down the device at voltages >4 V. If the shutdown function is not used, this pin can be connected to the VREF pin through a voltage divider.	See Figure 49
2	CHPF	Connect this pin to VPOS via a capacitor to determine the -3 dB point of the input signal high-pass filter. Only add a capacitor when operating at frequencies below 10 MHz.	See Figure 60
3, 10	VPOS	Supply for the Device. Connect these pins to a 5 V power supply. Pin 3 and Pin 10 are not internally connected; therefore, both must connect to the source.	N/A
4, 9, EPAD	COMM	System Common Connection. Connect these pins via low impedance to system common. The exposed paddle is also COMM and should have both a good thermal and good electrical connection to ground.	N/A
5	CLPF	Connection for Loop Filter Integration (Averaging) Capacitor. Connect a ground-referenced capacitor to this pin. A resistor can be connected in series with this capacitor to improve loop stability and response time. Minimum C_{LPF} value is 390 pF.	See Figure 51
6	VOUT	Output Pin in Measurement Mode (Error Amplifier Output). In measurement mode, this pin is connected to VSET. This pin can be used to drive a gain control when the device is used in controller mode.	See Figure 51
7	VSET	The voltage applied to this pin sets the decibel value of the required RF input voltage that results in zero current flow in the loop integrating capacitor pin, CLPF. This pin controls the variable gain amplifier (VGA) gain such that a 50 mV change in VSET reduces the gain by approximately 1 dB.	See Figure 50
8	TEMP	Temperature Sensor Output.	See Figure 45
11	VREF	General-Purpose Reference Voltage Output of 2.3 V.	See Figure 46
12	VTGT	The voltage applied to this pin determines the target power at the input of the RF squaring circuit. The intercept voltage is proportional to the voltage applied to this pin. The use of a lower target voltage increases the crest factor capacity; however, this may affect the system loop response.	See Figure 52
13	NC	No Connect.	N/A
14	INHI	This is the RF input pin for frequencies up to and including 2.6 GHz. The RF input signal is normally ac-coupled to this pin through a coupling capacitor.	See Figure 44
15	INLO	This is the RF input pin for frequencies above 2.6 GHz. The RF input signal is normally ac-coupled to this pin through a coupling capacitor.	See Figure 44
16	TCM1	This pin is used to adjust the intercept temperature compensation. Connect this pin to VREF through a voltage divider or to an external dc source.	See Figure 48

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{POS} = 5\text{ V}$, $Z_O = 50\ \Omega$, single-ended input drive, V_{OUT} connected to V_{SET} , $V_{TGT} = 1.4\text{ V}$, $C_{LPF} = 3.9\text{ nF}$, $C_{HPF} = 2.7\text{ nF}$, $T_A = +25^\circ\text{C}$ (black), -40°C (blue), $+85^\circ\text{C}$ (red), where appropriate. Error referred to best-fit line (linear regression) from -20 dBm to -40 dBm , unless otherwise indicated. Input RF signal is a sine wave (CW), unless otherwise indicated.

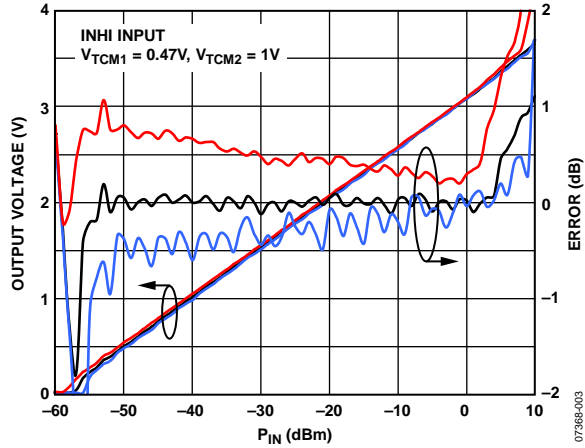


Figure 3. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 100 MHz, CW, Typical Device

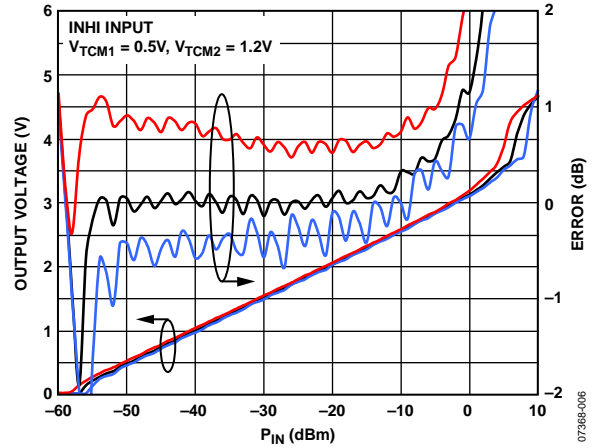


Figure 6. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 900 MHz, CW, Typical Device

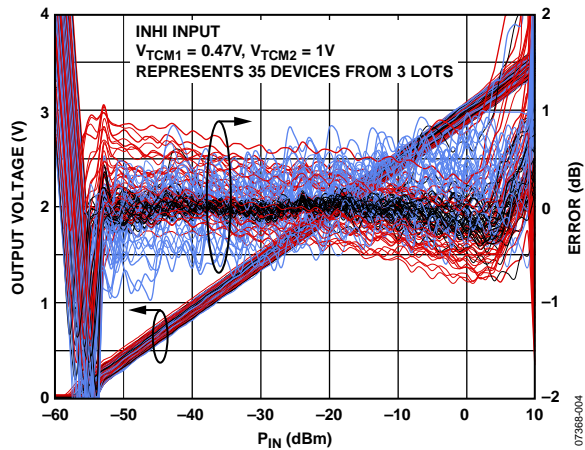


Figure 4. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 100 MHz, CW

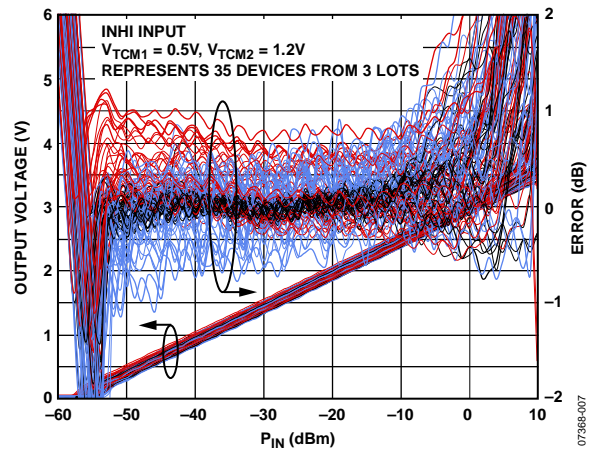


Figure 7. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 900 MHz, CW

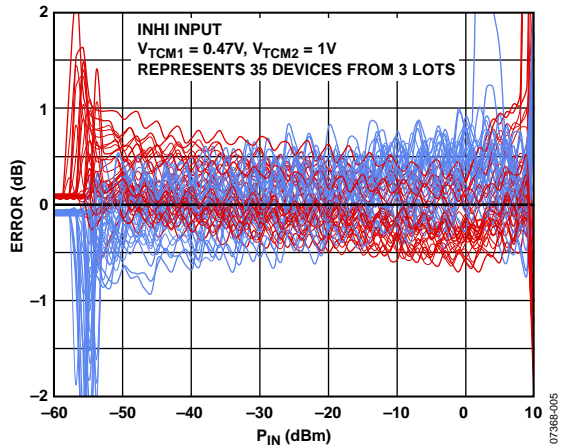


Figure 5. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude at 100 MHz, CW

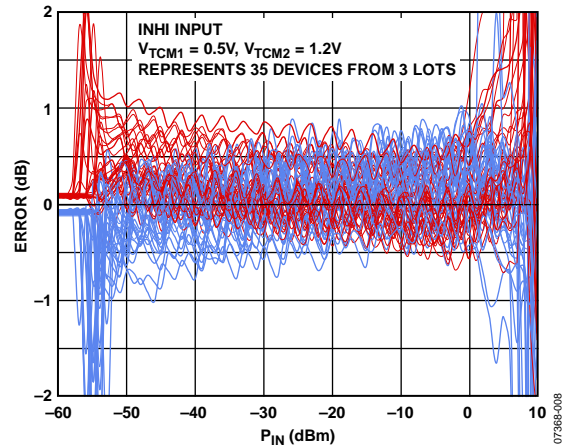


Figure 8. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude at 900 MHz, CW

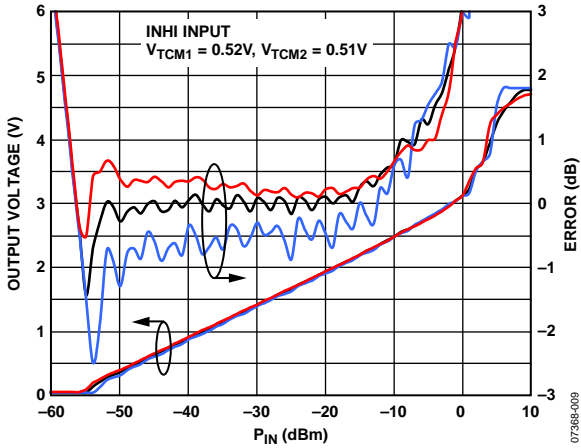


Figure 9. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 1.90 GHz, CW, Typical Device

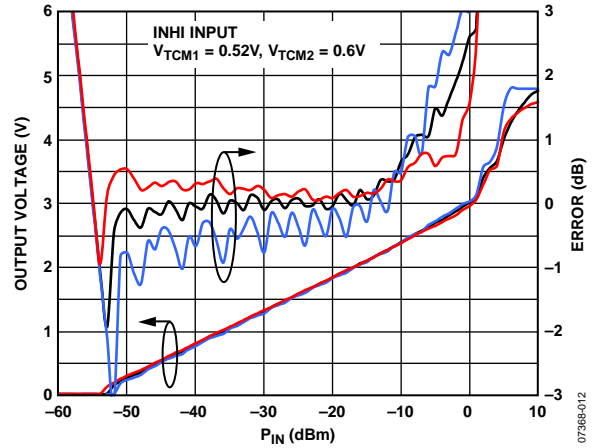


Figure 12. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.14 GHz, CW, Typical Device

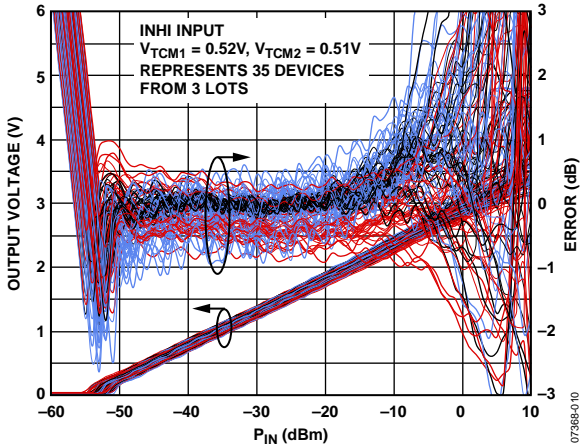


Figure 10. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 1.90 GHz, CW

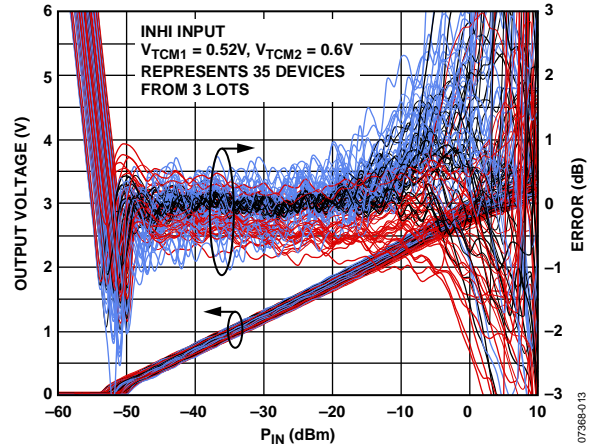


Figure 13. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.14 GHz, CW

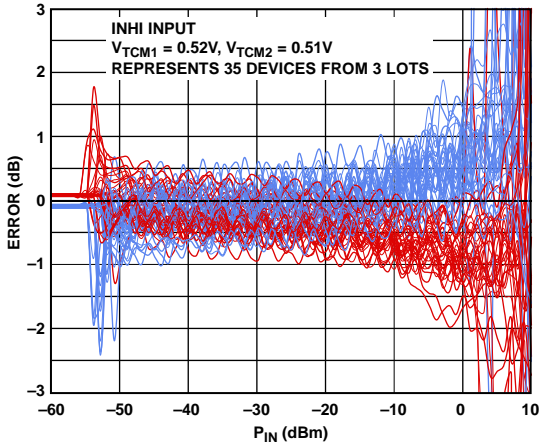


Figure 11. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude at 1.90 GHz, CW

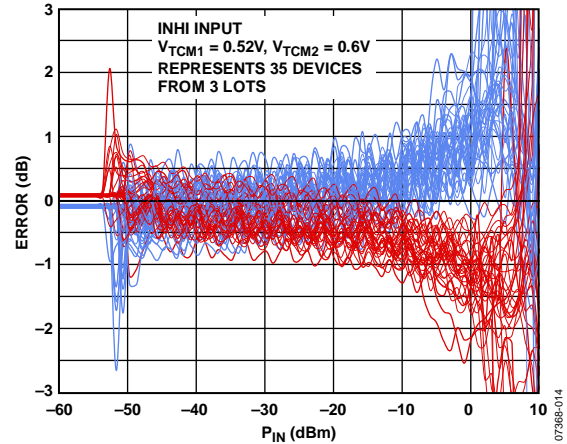


Figure 14. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude at 2.14 GHz, CW

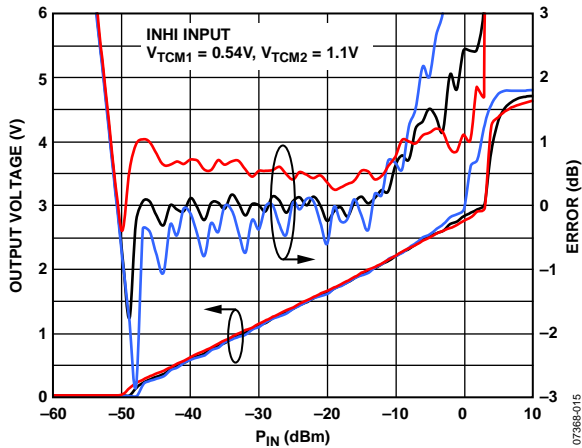


Figure 15. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.6 GHz, CW, Typical Device

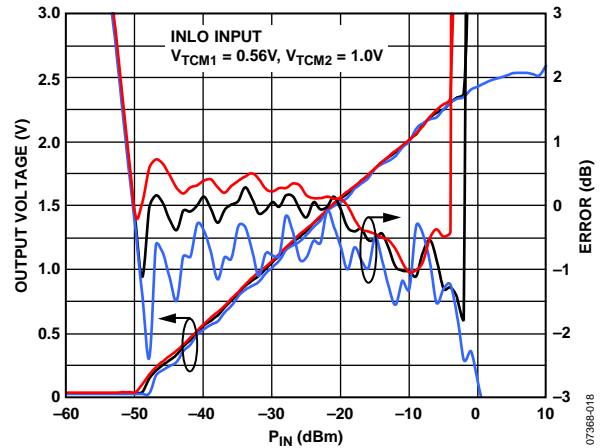


Figure 18. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 3.8 GHz, CW, Typical Device

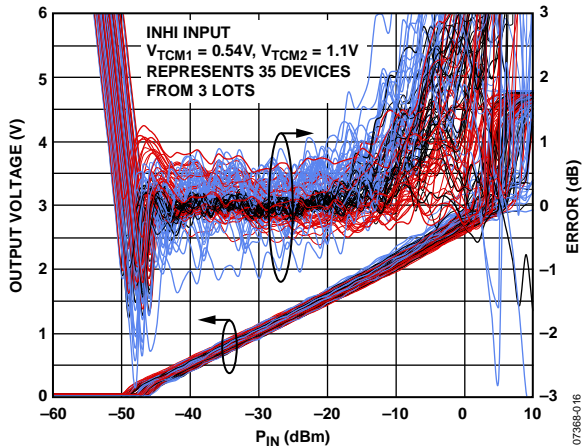


Figure 16. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 2.6 GHz, CW

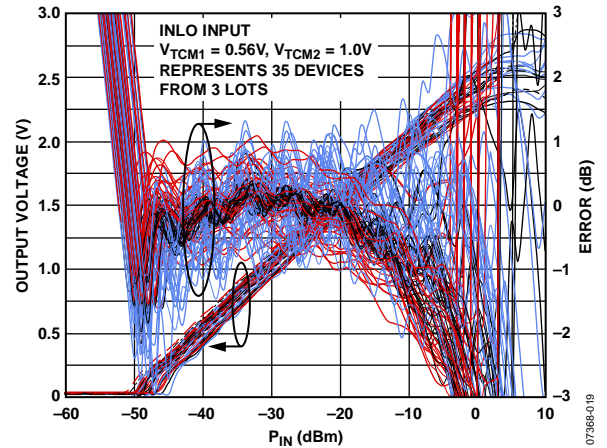


Figure 19. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 3.8 GHz, CW

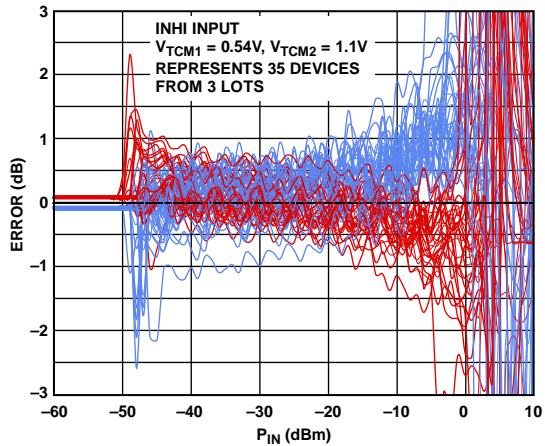


Figure 17. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude at 2.6 GHz, CW

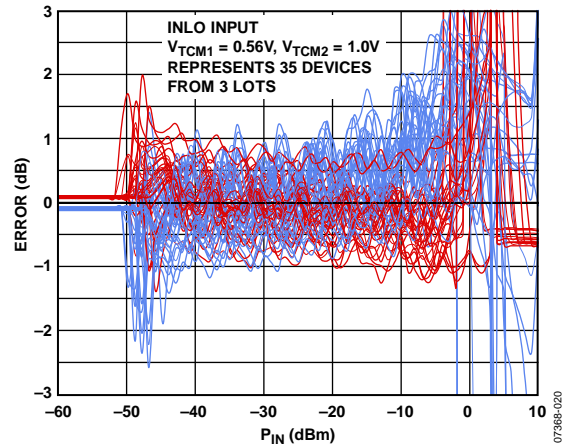


Figure 20. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude at 3.8 GHz, CW

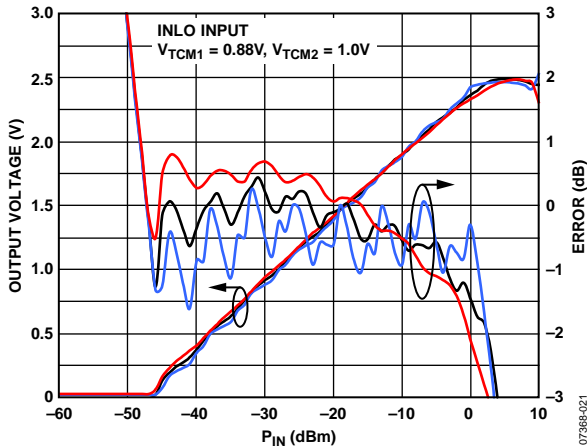


Figure 21. V_{OUT} and Log Conformance Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 5.8 GHz, Typical Device

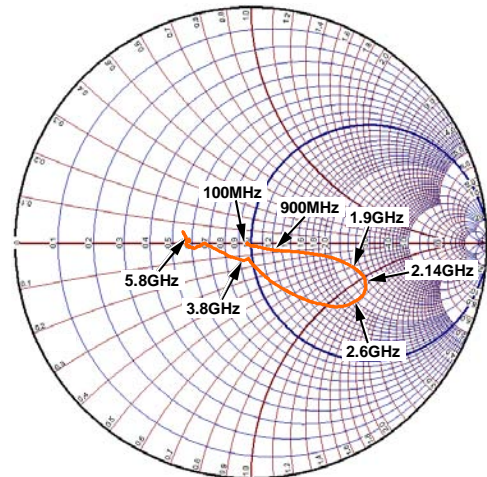


Figure 24. Single-Ended Input Impedance (S_{11}) vs. Frequency; $Z_0 = 50 \Omega$, INHI or INLO

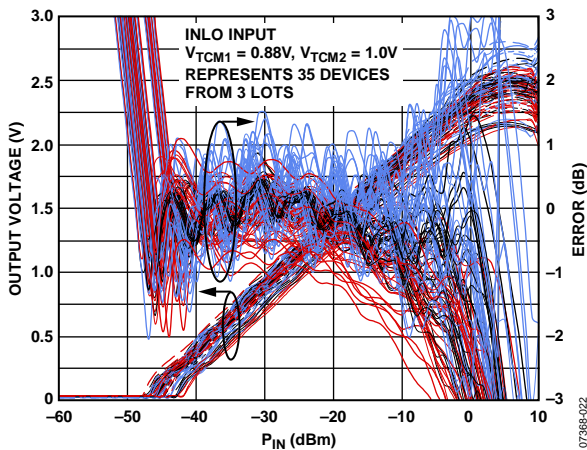


Figure 22. Distribution of V_{OUT} and Error with Respect to 25°C Ideal Line over Temperature vs. Input Amplitude at 5.8 GHz, CW

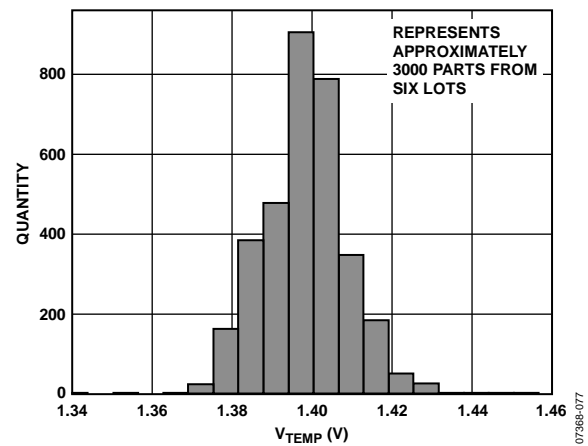


Figure 25. Distribution of V_{TEMP} Voltage at 25°C, No RF Input

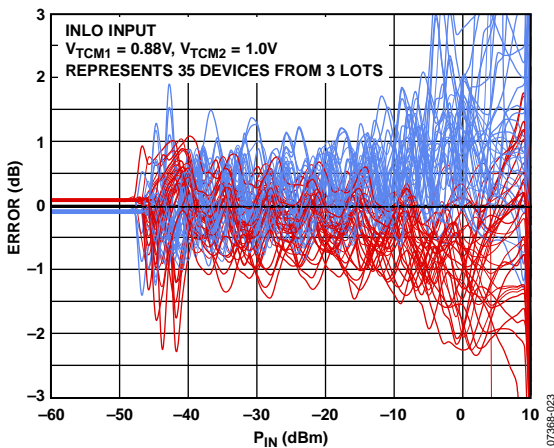


Figure 23. Distribution of Error with Respect to 25°C over Temperature vs. Input Amplitude at 5.8 GHz, CW

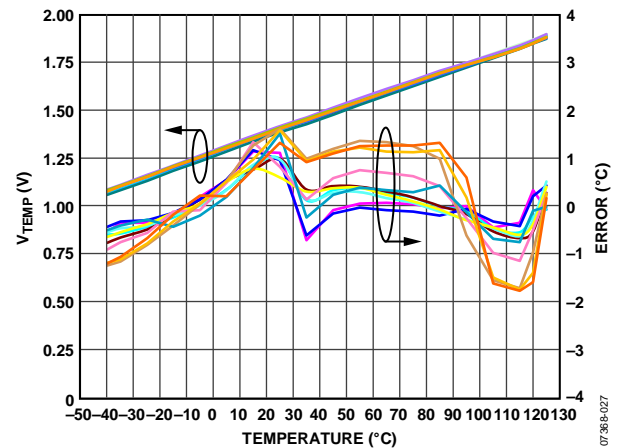


Figure 26. V_{TEMP} and Error with Respect to Straight Line vs. Temperature for Eleven Devices

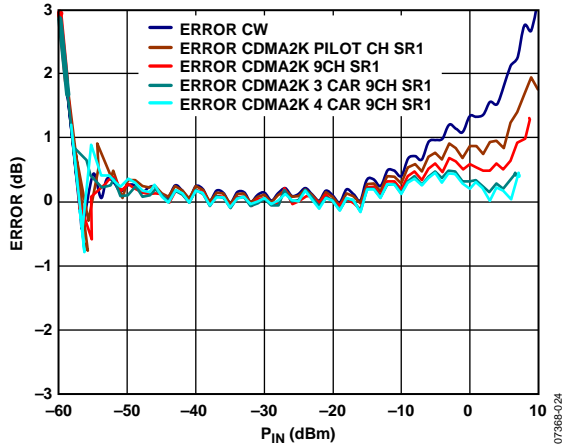


Figure 27. Error from CW Linear Reference vs. Input Amplitude with Modulation, Frequency at 900 MHz, $C_{LPF} = 0.1 \mu F$, INHI Input

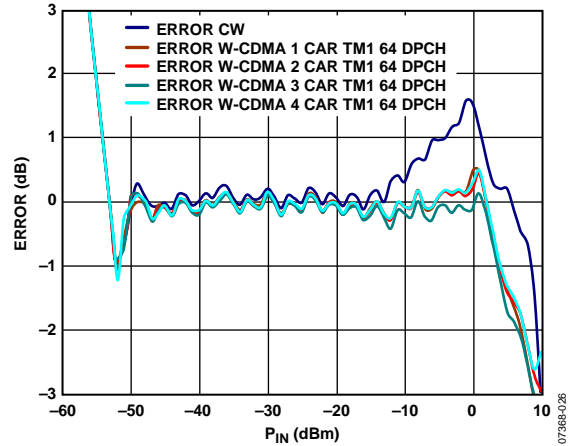


Figure 30. Error from CW Linear Reference vs. Input Amplitude with Modulation, Frequency at 2.14 GHz, $C_{LPF} = 0.1 \mu F$, INHI Input

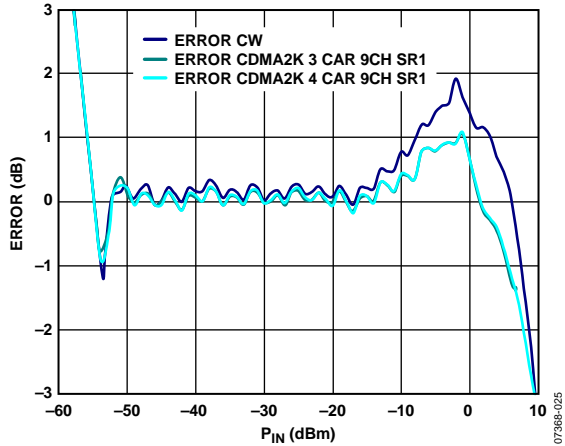


Figure 28. Error from CW Linear Reference vs. Input Amplitude with Modulation, Frequency at 1.9 GHz, $C_{LPF} = 0.1 \mu F$, INHI Input

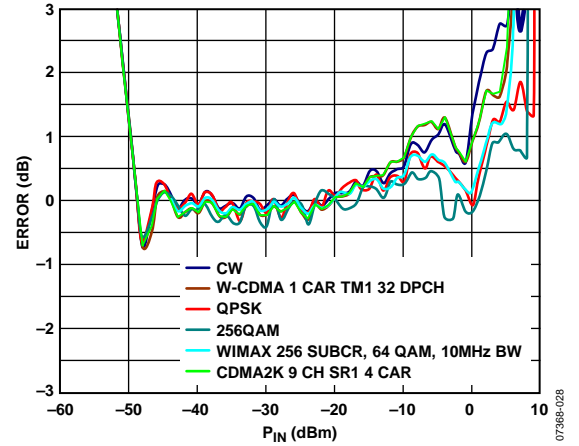


Figure 31. Error from CW Linear Reference vs. Input Amplitude with Modulation, Frequency at 2.6 GHz, $C_{LPF} = 0.1 \mu F$, INHI Input

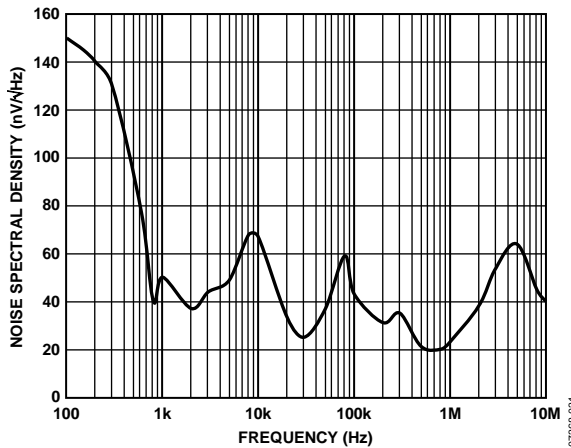


Figure 29. Typical Noise Spectral Density of V_{OUT} ; All C_{LPF} Values

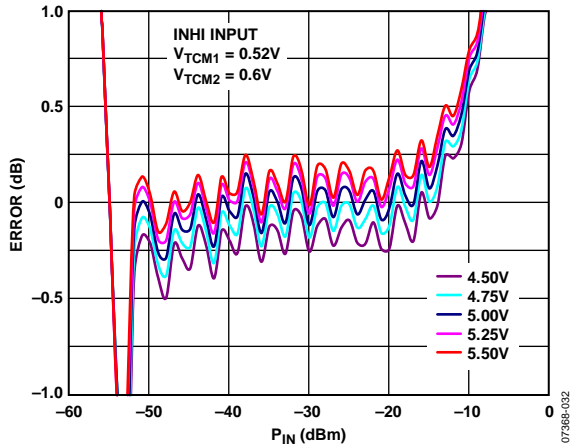


Figure 32. Output Stability at 2.14 GHz with V_{POS} Variation, Error Normalized to Response at 5 V, $V_{TGT} = 1.4 V$ (Fixed)

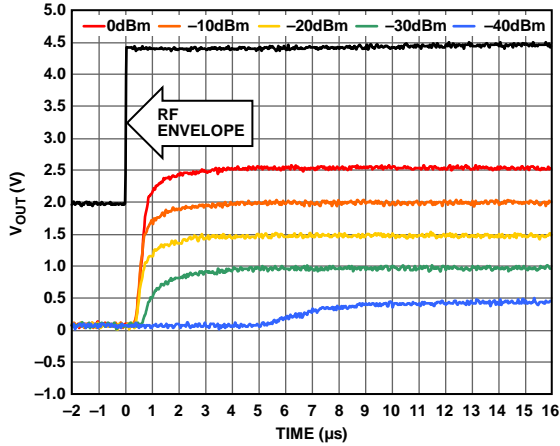


Figure 33. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, $C_{LPF} = 390 \text{ pF}$, $C_{HPF} = \text{Open}$, Rising Edge

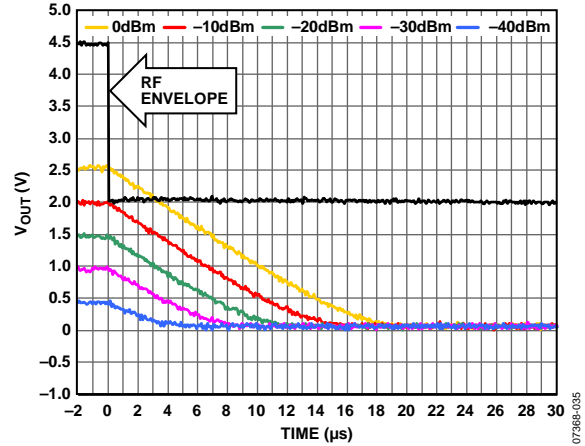


Figure 36. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, $C_{LPF} = 390 \text{ pF}$, $C_{HPF} = \text{Open}$, Falling Edge

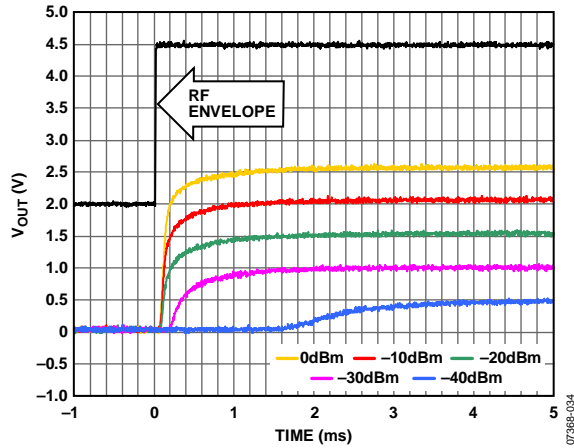


Figure 34. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, $C_{LPF} = 0.1 \text{ μF}$, $C_{HPF} = \text{Open}$, Rising Edge

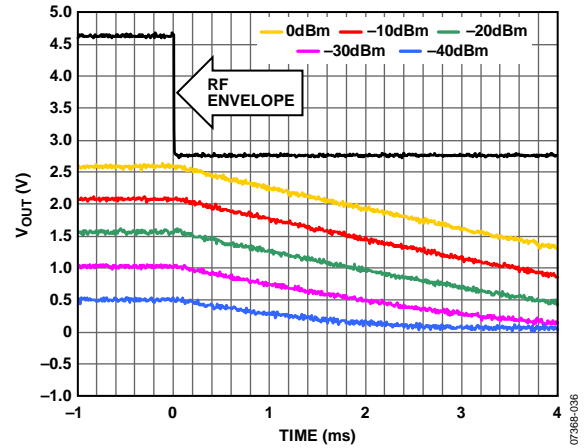


Figure 37. Output Response to RF Burst Input, Carrier Frequency at 2.14 GHz, $C_{LPF} = 0.1 \text{ μF}$, $C_{HPF} = \text{Open}$, Falling Edge

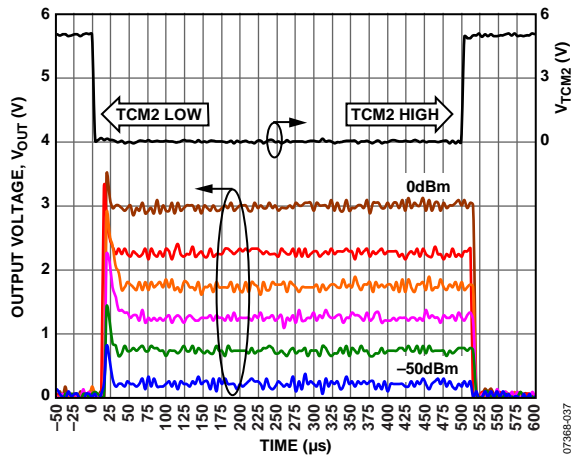


Figure 35. Output Response Using Power-Down Mode for Various RF Input Levels Carrier Frequency at 2.14 GHz, $C_{LPF} = 470 \text{ pF}$, $C_{HPF} = 220 \text{ pF}$

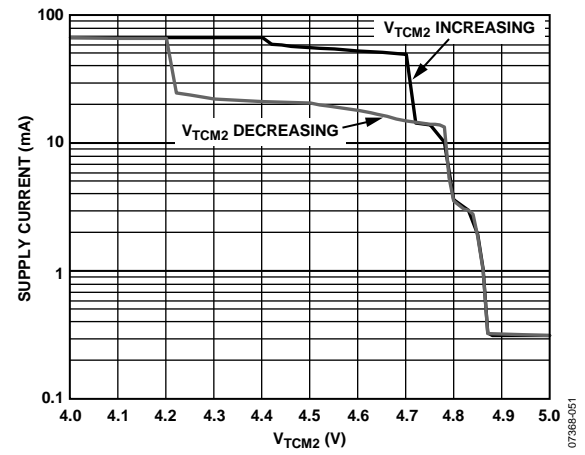


Figure 38. Supply Current vs. V_{TCM2}

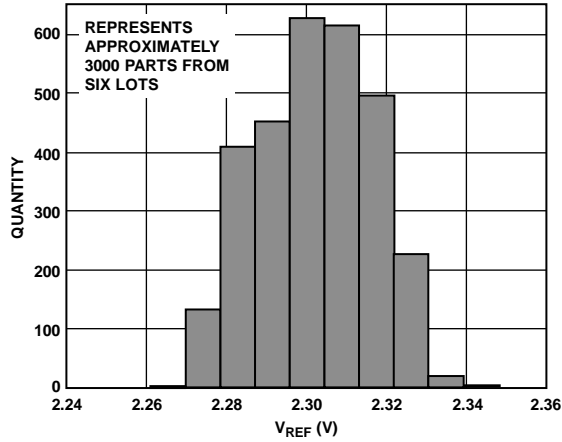


Figure 39. Distribution of V_{REF} , 25°C, No RF Input

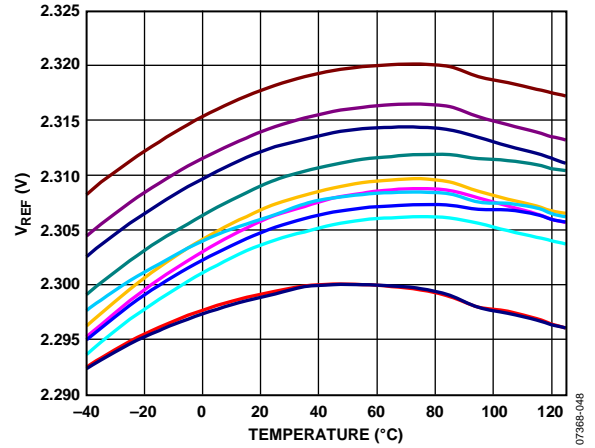


Figure 41. Change in V_{REF} with Temperature for Eleven Devices

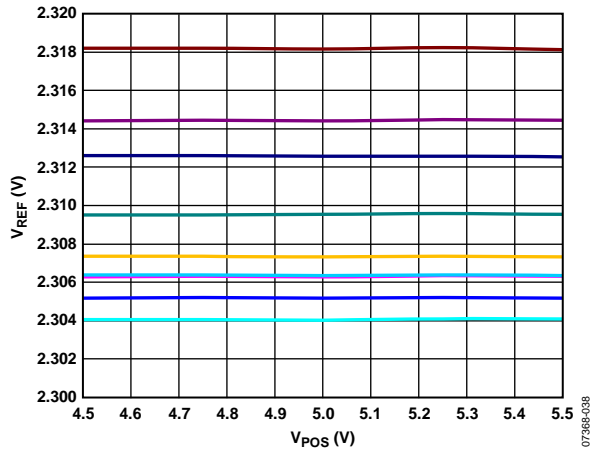


Figure 40. Change in V_{REF} with V_{POS} for Nine Devices

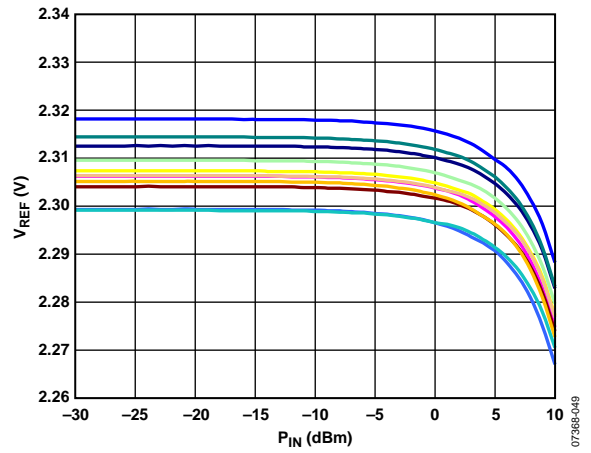


Figure 42. Change in V_{REF} with Input Amplitude for Eleven Devices

THEORY OF OPERATION

The AD8363 is a 6 GHz, true rms responding detector with a 40 dB measurement range at 6 GHz and a greater than 50 dB measurement range at frequencies less than 1 GHz. It incorporates a modified AD8362 architecture that increases the frequency range and improves measurement accuracy at high frequencies. Log conformance peak-to-peak ripple has been reduced to ± 0.1 dB over the entire dynamic range. Temperature stability of the rms output measurements provides ± 0.5 dB error typically over the specified temperature range of -40°C to 85°C through proprietary techniques.

The AD8363 is an rms-to-dc converter capable of operating on signals of approximately 50 Hz to 6 GHz or more. Unlike logarithmic amplifiers, the AD8363 response is waveform independent. The device accurately measures waveforms that have a high peak-to-rms ratio (crest factor).

The AD8363 consists of a high performance AGC loop. As shown in Figure 43, the AGC loop comprises a wide bandwidth variable gain amplifier (VGA), square law detectors, an amplitude target circuit, and an output driver. For a more detailed description of the functional blocks, see the AD8362 data sheet.

The nomenclature used in this data sheet to distinguish between a pin name and the signal on that pin is as follows:

- The pin name is all upper cased, for example, VPOS, COMM, and VOUT.
- The signal name or a value associated with that pin is the pin mnemonic with a partial subscript, for example, C_{LPF} , C_{HPF} , and V_{OUT} .

SQUARE LAW DETECTOR AND AMPLITUDE TARGET

The VGA gain has the form

$$G_{SET} = G_O \exp(-V_{SET}/V_{GNS}) \quad (1)$$

where:

G_O is the basic fixed gain.

V_{GNS} is a scaling voltage that defines the gain slope (the decibel change per voltage). The gain decreases with increasing V_{SET} .

The VGA output is

$$V_{SIG} = G_{SET} \times RF_{IN} = G_O \times RF_{IN} \exp(V_{SET}/V_{GNS}) \quad (2)$$

where

RF_{IN} is the ac voltage applied to the input terminals of the AD8363.

The output of the VGA, V_{SIG} , is applied to a wideband square law detector. The detector provides the true rms response of the RF input signal, independent of waveform. The detector output, I_{SQR} , is a fluctuating current with positive mean value. The difference between I_{SQR} and an internally generated current, I_{TGT} , is integrated by C_F and the external capacitor attached to the CLPF pin at the summing node. C_F is an on-chip 25 pF filter capacitor, and C_{LPF} , the external capacitance connected to the CLPF pin, can be used to arbitrarily increase the averaging time while trading off with the response time. When the AGC loop is at equilibrium

$$\text{Mean}(I_{SQR}) = I_{TGT} \quad (3)$$

This equilibrium occurs only when

$$\text{Mean}(V_{SIG}^2) = V_{TGT}^2 \quad (4)$$

where V_{TGT} is the voltage presented at the VTGT pin. This pin can conveniently be connected to the VREF pin through a voltage divider to establish a target rms voltage V_{ATG} of ~ 70 mV rms, when $V_{TGT} = 1.4$ V.

Because the square law detectors are electrically identical and well matched, process and temperature dependant variations are effectively cancelled.

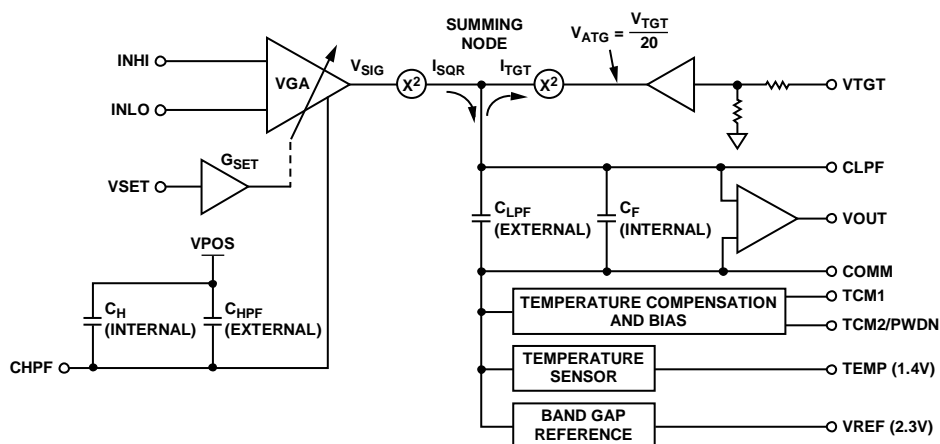


Figure 43. Simplified Architecture Details

By forcing the previous identity through varying the VGA setpoint, it is apparent that

$$\text{RMS}(V_{\text{SIG}}) = \sqrt{\text{Mean}(V_{\text{SIG}}^2)} = \sqrt{(V_{\text{ATG}})^2} = V_{\text{ATG}} \quad (5)$$

Substituting the value of V_{SIG} from Equation 2 results in

$$\text{RMS}(G_0 \times \text{RF}_{\text{IN}} \exp(-V_{\text{SET}}/V_{\text{GNS}})) = V_{\text{ATG}} \quad (6)$$

When connected as a measurement device, $V_{\text{SET}} = V_{\text{OUT}}$. Solving for V_{OUT} as a function of RF_{IN}

$$V_{\text{OUT}} = V_{\text{SLOPE}} \times \log_{10}(\text{RMS}(\text{RF}_{\text{IN}})/V_Z) \quad (7)$$

where:

V_{SLOPE} is 1 V/decade (or 50 mV/dB).

V_Z is the intercept voltage.

When $\text{RMS}(\text{RF}_{\text{IN}}) = V_Z$, because $\log_{10}(1) = 0$, this implies that $V_{\text{OUT}} = 0$ V, making the intercept the input that forces $V_{\text{OUT}} = 0$ V. V_Z has been fixed to approximately 280 μV (approximately -58 dBm, referred to 50 Ω) with a CW signal at 100 MHz. In reality, the AD8363 does not respond to signals less than ~ -56 dBm. This means that the intercept is an extrapolated value outside the operating range of the device.

If desired, the effective value of V_{SLOPE} can be altered by using a resistor divider between V_{OUT} and V_{SET} . (Refer to the Altering the Slope section for more information.)

In most applications, the AGC loop is closed through the setpoint interface and the V_{SET} pin. In measurement mode, V_{OUT} is directly connected to V_{SET} . (See the Measurement Mode Basic Connections section for more information.) In controller mode, a control voltage is applied to V_{SET} and the V_{OUT} pin typically drives the control input of an amplification or attenuation system. In this case, the voltage at the V_{SET} pin forces a signal amplitude at the RF inputs of the AD8363 that balances the system through feedback. (See the Controller Mode Basic Connections section for more information.)

RF INPUT INTERFACE

Figure 44 shows the connections of the RF inputs within the AD8363. The input impedance is set primarily by an internal 50 Ω resistor connected between INHI and INLO. A dc level of approximately half the supply voltage on each pin is established internally. Either the INHI pin or the INLO pin can be used as the single-ended RF input pin. (See the Choice of RF Input Pin section.) If the dc levels at these pins are disturbed, performance is compromised; therefore, signal coupling capacitors must be connected from the input signal to INHI and INLO. The input signal high-pass corner formed by the coupling capacitors and the internal resistances is

$$f_{\text{HIGH-PASS}} = 1/(2 \times \pi \times 50 \times C) \quad (8)$$

where C is in farads and $f_{\text{HIGH-PASS}}$ is in hertz. The input coupling capacitors must be large enough in value to pass the input signal frequency of interest. The other input pin should be RF ac-coupled to common (ground).

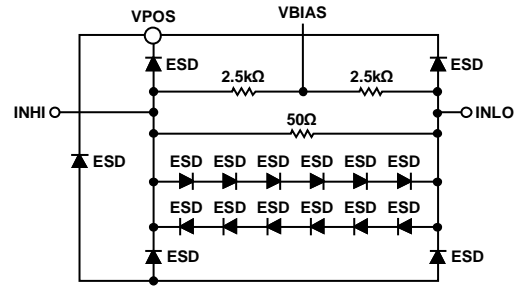


Figure 44. RF Inputs Simplified Schematic

Extensive ESD protection is employed on the RF inputs, which limits the maximum possible input amplitude to the AD8363.

CHOICE OF RF INPUT PIN

The dynamic range of the AD8363 can be optimized by choosing the correct RF input pin for the intended frequency of operation. Using INHI (Pin 14), users can obtain the best dynamic range at frequencies up to 2.6 GHz. Above 2.6 GHz, it is recommended that INLO (Pin 15) be used. At 2.6 GHz, the performance obtained at the two inputs is approximately equal. The AD8363 was designed with a single-ended RF drive in mind. A balun can be used to drive INHI and INLO differentially, but it is not necessary, and it does not result in improved dynamic range.

SMALL SIGNAL LOOP RESPONSE

The AD8363 uses a VGA in a loop to force a squared RF signal to be equal to a squared dc voltage. This nonlinear loop can be simplified and solved for a small signal loop response. The low-pass corner pole is given by

$$\text{Freq}_{\text{LP}} \approx 1.83 \times I_{\text{TGT}}/(C_{\text{LPF}}) \quad (9)$$

where:

I_{TGT} is in amperes.

C_{LPF} is in farads.

Freq_{LP} is in hertz.

I_{TGT} is derived from V_{TGT} ; however, I_{TGT} is a squared value of V_{TGT} multiplied by a transresistance, namely

$$I_{\text{TGT}} = g_m \times V_{\text{TGT}}^2 \quad (10)$$

g_m is approximately 18.9 μS , so with V_{TGT} equal to the typically recommended 1.4 V, I_{TGT} is approximately 37 μA . The value of this current varies with temperature; therefore, the small signal pole varies with temperature. However, because the RF squaring circuit and dc squaring circuit track with temperature, there is no temperature variation contribution to the absolute value of V_{OUT} .

For CW signals,

$$\text{Freq}_{\text{LP}} \approx 67.7 \times 10^{-6}/(C_{\text{LPF}}) \quad (11)$$

However, signals with large crest factors include low pseudorandom frequency content that either needs to be filtered out or sampled and averaged out. See the Choosing a Value for C_{LPF} section for more information.

TEMPERATURE SENSOR INTERFACE

The AD8363 provides a temperature sensor output with an output voltage scaling factor of approximately 5 mV/°C. The output is capable of sourcing 4 mA and sinking 50 μA maximum at temperatures at or above 25°C. If additional current sink capability is desired, an external resistor can be connected between the TEMP and COMM pins. The typical output voltage at 25°C is approximately 1.4 V.

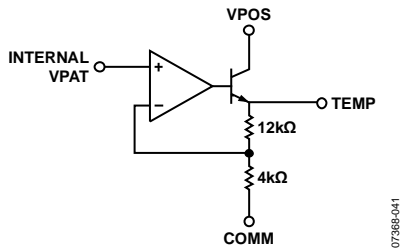


Figure 45. TEMP Interface Simplified Schematic

VREF INTERFACE

The VREF pin provides an internally generated voltage reference. The V_{REF} voltage is a temperature stable 2.3 V reference that is capable of sourcing 4 mA and sinking 50 μA maximum at temperatures at or above 25°C. An external resistor can be connected between the VREF and COMM pins to provide additional current sink capability. The voltage on this pin can be used to drive the TCM1, TCM2/PWDN, and VTGT pins, if desired.

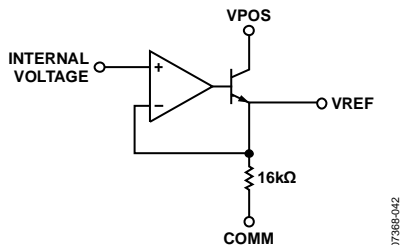


Figure 46. VREF Interface Simplified Schematic

TEMPERATURE COMPENSATION INTERFACE

While the AD8363 has a highly stable measurement output with respect to temperature, it uses proprietary techniques to make it even more stable. For optimal performance, the output temperature drift must be compensated for using the TCM1 and TCM2/PWDN pins. The absolute value of compensation varies with frequency and V_{TGT} . Table 4 shows the recommended voltages for the TCM1 and TCM2/PWDN pins to maintain the best temperature drift error over the rated temperature range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$) when driven single-ended and using a $V_{TGT} = 1.4\text{ V}$.

Table 4. Recommended Voltages for TCM1 and TCM2/PWDN

Frequency	TCM1 (V)	TCM2/PWDN (V)
100 MHz	0.47	1.0
900 MHz	0.5	1.2
1.9 GHz	0.52	0.51
2.14 GHz	0.52	0.6
2.6 GHz	0.54	1.1
3.8 GHz	0.56	1.0
5.8 GHz	0.88	1.0

The values in Table 4 were chosen to give the best drift performance at the high end of the usable dynamic range over the -40°C to $+85^{\circ}\text{C}$ temperature range.

Compensating the device for the temperature drift using TCM1 and TCM2/PWDN allows for great flexibility and the user may wish to modify these values to optimize for another amplitude point in the dynamic range, for a different temperature range, or for an operating frequency other than those shown in Table 4.

To find a new compensation point, V_{TCM1} and V_{TCM2} can be swept while monitoring V_{OUT} over the temperature at the frequency and amplitude of interest. The optimal voltages for V_{TCM1} and V_{TCM2} to achieve minimum temperature drift at a given power and frequency are the values of V_{TCM1} and V_{TCM2} where V_{OUT} has minimum movement. See the AD8364 and ADL5513 data sheets for more information.

Varying V_{TCM1} and V_{TCM2} has only a very slight effect on V_{OUT} at device temperatures near 25°C; however, the compensation circuit has more and more effect, and is more and more necessary for best temperature drift performance, as the temperature departs farther from 25°C.

Figure 47 shows the effect on temperature drift performance at 25°C and 85°C as V_{TCM1} is varied but V_{TCM2} is held constant at 0.6 V.

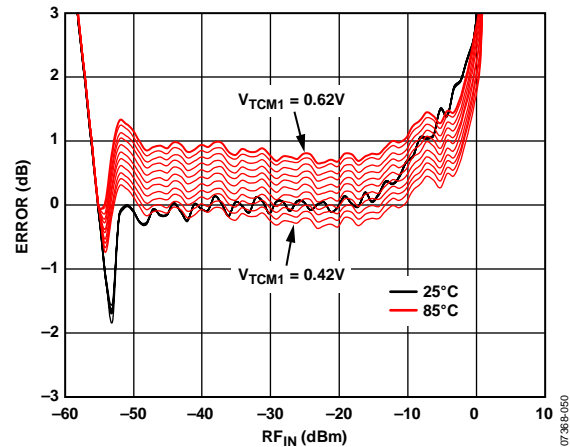


Figure 47. Error vs. Input Amplitude over Stepped V_{TCM1} Values, 25°C and 85°C, 2.14 GHz, $V_{TCM2} = 0.6\text{ V}$

TCM1 primarily adjusts the intercept of the AD8363 at temperature. In this way, TCM1 can be thought of as a coarse adjustment to the compensation. Conversely, TCM2 performs a fine adjustment. For this reason, it is advised that when searching for compensation with V_{TCM1} and V_{TCM2} , that V_{TCM1} be adjusted first, and when best performance is found, V_{TCM2} can then be adjusted for optimization.

It is evident from Figure 47 that the temperature compensation circuit can be used to adjust for the lowest drift at any input amplitude of choice. Though not shown in Figure 47, a similar analysis can simultaneously be performed at -40°C , or any other temperature within the operating range of the AD8363.

Performance varies slightly from device to device; therefore, optimal V_{TCM1} and V_{TCM2} values must be arrived at statistically over a population of devices to be useful in mass production applications.

The TCM1 and TCM2 pins have high input impedances, approximately 5 k Ω and 500 k Ω , respectively, and can be conveniently driven from an external source or from a fraction of V_{REF} by using a resistor divider. V_{REF} does change slightly with temperature and RF input amplitude (see Figure 41 and Figure 42); however, the amount of change is unlikely to result in a significant effect on the final temperature stability of the RF measurement system.

Figure 48 shows a simplified schematic representation of TCM1. See the Power-Down Interface section for the TCM2 interface.

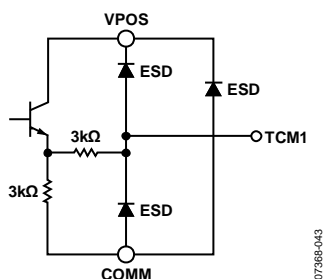


Figure 48. TCM1 Interface Simplified Schematic

POWER-DOWN INTERFACE

The quiescent and disabled currents for the AD8363 at 25°C are approximately 60 mA and 300 μ A, respectively. The dual function pin, TCM2/PWDN, is connected to a temperature compensation circuit as well as a power-down circuit. Typically, when PWDN is greater than $V_{POS} - 0.1$ V, the device is fully powered down. Figure 38 shows this characteristic as a function of V_{PWDN} . Note that because of the design of this section of the AD8363, as V_{TCM2} passes through a narrow range at ~ 4.5 V (or $\sim V_{POS} - 0.5$ V), the TCM2/PWDN pin sinks approximately 750 μ A. The source used to disable the AD8363 must have a sufficiently high current capability for this reason. Figure 35 shows the typical response times for various RF input levels. The output reaches within 0.1 dB of its steady-state value in approximately 35 μ s; however, the reference voltage is available to full accuracy in a much shorter time. This wake-up response varies depending on the input coupling and the capacitances, C_{HPF} and C_{LPF} .

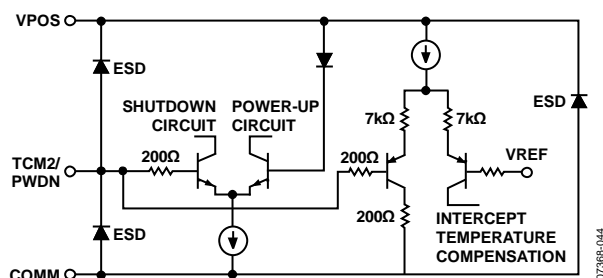


Figure 49. PWDN Interface Simplified Schematic

VSET INTERFACE

The VSET interface has a high input impedance of 72 k Ω . The voltage at VSET is converted to an internal current used to set the internal VGA gain. The VGA attenuation control is approximately 19 dB/V.

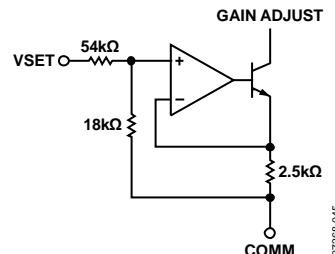


Figure 50. VSET Interface Simplified Schematic

OUTPUT INTERFACE

The output driver used in the AD8363 is different from the output stage on the AD8362. The AD8363 incorporates rail-to-rail output drivers with pull-up and pull-down capabilities. The closed-loop -3 dB bandwidth of the VOUT buffer with no load is approximately 58 MHz with a single-pole roll-off of -20 dB/dec. The output noise is approximately 45 nV/ $\sqrt{\text{Hz}}$ at 100 kHz, which is independent of C_{LPF} due to the architecture of the AD8363. VOUT can source and sink up to 10 mA. There is an internal load between VOUT and COMM of 2.5 k Ω .

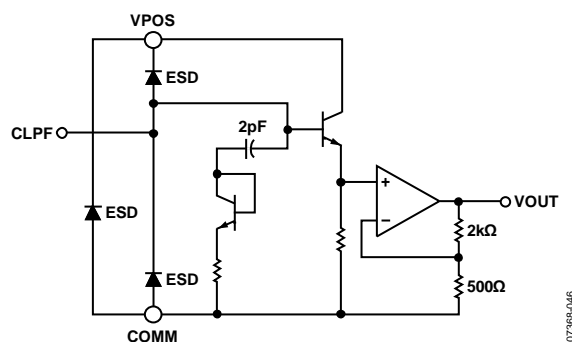


Figure 51. VOUT Interface Simplified Schematic

VTGT INTERFACE

The target voltage can be set with an external source or by connecting the VREF pin (nominally 2.3 V) to the VTGT pin through a resistive voltage divider. With 1.4 V on the VTGT pin, the rms voltage that must be provided by the VGA to balance the AGC feedback loop is $1.4 \text{ V} \times 0.05 = 70 \text{ mV rms}$. Most of the characterization information in this data sheet was collected at $V_{TGT} = 1.4 \text{ V}$. Voltages higher and lower than this can be used; however, doing so increases or decreases the gain at the internal squaring cell, which results in a corresponding increase or decrease in intercept. This in turn affects the sensitivity and the usable measurement range. Because the gain of the squaring cell varies with temperature, oscillations or a loss in measurement range can result. For these reasons, do not reduce V_{TGT} below 1.3 V.

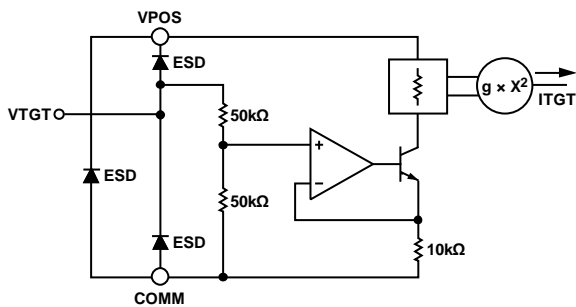


Figure 52. VTGT Interface Simplified Schematic

OPERATION TO 125°C

Most of the information in this data sheet describes operation up to, but not exceeding, 85°C. Operation up to 125°C is possible; however, the performance of the AD8363 above 85°C can be degraded. Figure 53 shows the typical operation at 125°C as compared to other temperatures using the TCM1 and TCM2 values in Table 4. Temperature compensation can be optimized for operation above 85°C by modifying the voltages on the TCM1 and TCM2 pins from those shown in Table 4.

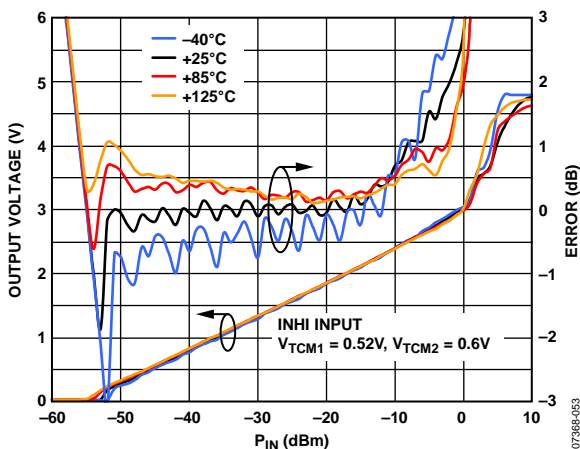


Figure 53. V_{OUT} and Log Conformance Error vs. Input Amplitude at 2.14 GHz, -40°C to $+125^\circ\text{C}$

BASIS FOR ERROR CALCULATIONS

The slope and intercept used in the error plots are calculated using the coefficients of a linear regression performed on data collected in its central operating range. The error plots in the Typical Performance Characteristics section are shown in two formats: error from the ideal line and error with respect to 25°C. The error from the ideal line is the decibel difference in V_{OUT} from the ideal straight-line fit of V_{OUT} calculated by the linear-regression fit over the linear range of the detector, typically at 25°C. The error in decibels is calculated by

$$\text{Error (dB)} = (V_{OUT} - \text{Slope} \times (P_{IN} - P_Z)) / \text{Slope} \quad (12)$$

where P_Z is the x-axis intercept expressed in dBm (the input amplitude that produces a 0 V output, if such an output is possible).

The linear range of the detector was assumed to be -20 dBm to -40 dBm . The error from the ideal line is not a measure of absolute accuracy because it is calculated using the slope and intercept of each device. However, it verifies the linearity and the effect of temperature and modulation on the response of the device. Examples of this type of plot are Figure 3 and Figure 4. The slope and intercept that form the ideal line are those at 25°C with CW modulation. Figure 27, Figure 28, Figure 30, and Figure 31 show the error with various popular forms of modulation with respect to the ideal CW line. This method for calculating error is accurate assuming each device is calibrated at room temperature and/or CW modulation, as appropriate.

In the second plot format, the V_{OUT} voltage at a given input amplitude and temperature is subtracted from the corresponding V_{OUT} at 25°C and then divided by the 25°C slope to obtain an error in decibels. This type of plot does not provide any information on the linear-in-dB performance of the device; it merely shows the decibel equivalent of the deviation of V_{OUT} over temperature, given a calibration at 25°C. When calculating error from any one particular calibration point, this error format is accurate. It is accurate over the full range shown on the plot assuming enough calibration points are used. Figure 5 shows this plot type.

The error calculation for Figure 32 is in the same method as the first type previously mentioned, except that instead of varying the operating temperature of the device, the operating voltage was varied and the error is expressed with the nominal (5 V) response as the base response.

The error calculations for Figure 26 are similar to that for the V_{OUT} plots. The slope and intercept of the V_{TEMP} function vs. temperature were determined and applied as follows:

$$\text{Error } (^\circ\text{C}) = (V_{TEMP} - \text{Slope} \times (\text{Temp} - T_Z)) / \text{Slope} \quad (13)$$

where:

T_Z is the x-axis intercept expressed in degrees Celsius (the temperature that would result in a V_{TEMP} of 0 V (an extrapolation because this is not possible).

Temp is the temperature of the AD8363 in degrees Celsius. Slope is expressed in $\text{V}/^\circ\text{C}$.

V_{TEMP} is the voltage at the TEMP pin at that temperature.

MEASUREMENT MODE BASIC CONNECTIONS

The AD8363 requires a single supply of nominally 5 V. The supply is connected to the two supply pins, VPOS. Decouple the pins using two capacitors with values equal or similar to those shown in Figure 54. These capacitors must provide a low impedance over the full frequency range of the input, and they should be placed as close as possible to the VPOS pins. Use two different capacitor values in parallel to provide a broadband ac short to ground.

Input signals can be applied differentially or single-ended; however, in both cases, the input impedance is 50 Ω . Most performance information in this data sheet was derived with a single-ended drive. The optimal measurement range is achieved using a single-ended drive on the INHI pin at frequencies below 2.6 GHz (as shown in Figure 54), and likewise, optimal performance is achieved using the INLO pin above 2.6 GHz (similar to Figure 54; except INLO is ac-coupled to the input and INHI is ac-coupled to ground).

The AD8363 is placed in measurement mode by connecting VOUT to VSET. This closes the AGC loop within the device with V_{OUT} representing the VGA control voltage, which is required to present the correct rms voltage at the input of the internal square law detector.

As the input signal is swept over its nominal input dynamic range of -50 dBm to 0 dBm, the output swings from approximately 0 V to a high value of approximately 3 V.

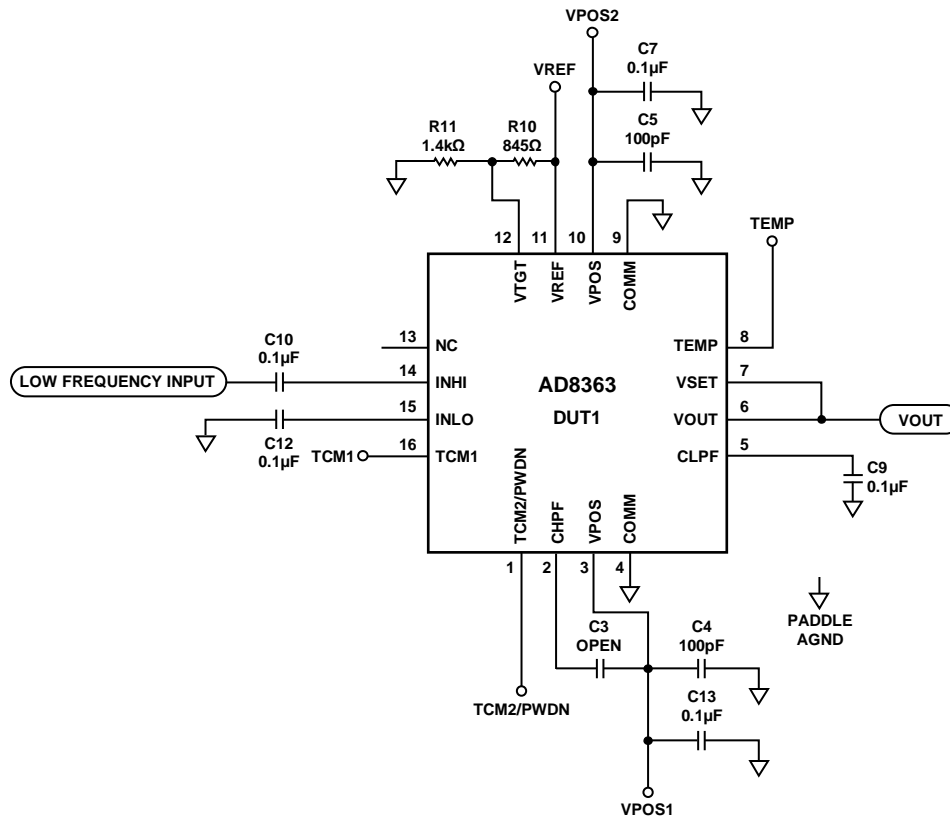


Figure 54. Measurement Mode Basic Connections

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DEVICE CALIBRATION AND ERROR CALCULATION

The measured transfer function of the AD8363 at 2.14 GHz is shown in Figure 55. It shows plots of both output voltage vs. input amplitude (power) and calculated error vs. input amplitude (power). As the input power varies from -50 dBm to 0 dBm, the output voltage varies from 0.25 V to about 2.8 V.

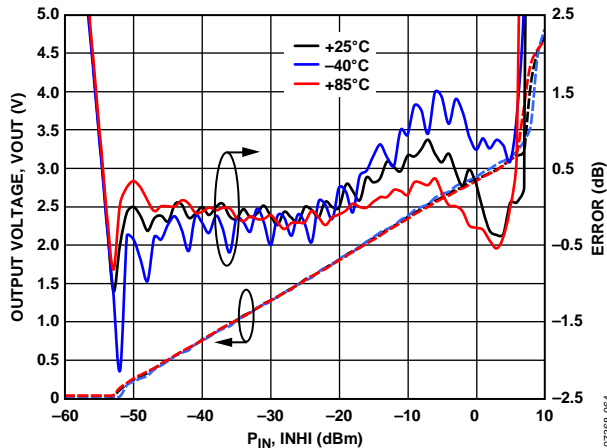


Figure 55. 2.14 GHz Transfer Function Using Two-Point Calibration

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. The equation for output voltage can be written as

$$V_{OUT} = Slope \times (P_{IN} - Intercept) \quad (14)$$

where:

Slope is the change in output voltage divided by the change in power (dB).

Intercept is the calculated input power level at which the output voltage would be 0 V. (Note that *Intercept* is a theoretical value; the output voltage can never achieve 0 V).

In general, calibration is performed by applying two (or more) known signal levels into the input of the AD8363 and by measuring the corresponding output voltages. The calibration points are generally within the linear-in-dB operating range of the device (see the Specifications section for more details).

The slope and intercept are calculated as follows:

$$Slope = (V_{OUT1} - V_{OUT2}) / (P_{IN1} - P_{IN2}) \quad (15)$$

$$Intercept = P_{IN1} - (V_{OUT1} / Slope) \quad (16)$$

The previous formula for intercept is a shorthand formula based upon Equation 14 and the assumption that the AD8363 is operating within the linear-in-dB operating range. When the slope and intercept are calculated, an equation can be written that allows the calculation of the ideal input power based on the output voltage of the detector.

$$P_{IN} (unknown) = (V_{OUT1(MEASURED)} / Slope) + Intercept \quad (17)$$

The log conformance error is the deviation of the detector from the ideal calculated power and is given by

$$Error (dB) = (V_{OUT(MEASURED)} - V_{OUT(IDEAL)}) / Slope \quad (18)$$

Figure 56 includes a plot of the error at 25°C , the temperature at which the log amp is calibrated. Note that the error is not zero because the detector does not perfectly follow the ideal straight line. The error at the calibration points (in this case, -40 dBm and -21 dBm) are, however, equal to zero by definition. Note that Figure 55 is slightly different from those found in the Typical Performance Characteristics section; its slope and intercept are calculated using a two-point calculation and not based on multiple points, as was used for the Typical Performance Characteristics.

Figure 55 also includes error plots for the output voltage at -40°C and $+85^{\circ}\text{C}$. These error plots are calculated using the slope and intercept at 25°C . Another way of saying this is that the hot and cold temperatures are calculated with respect to the output voltage at ambient, and by definition, the error at ambient becomes equal to 0 . This is consistent with calibration in a mass production environment, where calibration at temperature is not practical.

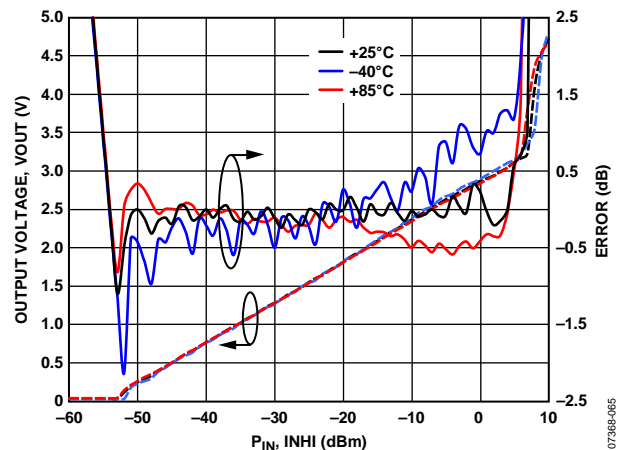


Figure 56. 2.14 GHz Transfer Function Using a Three-Point Calibration

SELECTING AND INCREASING CALIBRATION POINTS TO IMPROVE ACCURACY OVER A REDUCED RANGE

Choose the amount and location of the calibration points carefully because they can optimize the performance of the detector. In some applications, increasing the dynamic range of the AD8363 may be desirable; however, in others, very high accuracy is required at one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power. These objectives can be achieved by the proper selection of the amount and location of the calibration points.

Increasing the amount of calibration points can increase the accuracy of the room temperature performance over a select power level. Figure 56 shows the same measured data as Figure 55; except that one calibration point was added at -7 dBm giving an increase in room temperature linearity between -20 dBm to $+4$ dBm. Figure 56 is similar to Figure 14, except Figure 14 includes more parts and assumes many more calibration points, specifically 1 dB steps from -20 dBm to -40 dBm.

Even though a large amount of calibration points is less practical, Figure 14 is helpful because it shows the true temperature performance no matter the location of the calibration point. As can be seen from both Figure 14 and Figure 56, the temperature performance tends to change at power levels above -15 dBm. As shown in Figure 14, because the distribution of temperature performance is tight for the higher power levels, V_{TCM1} and V_{TCM2} can be optimized for the higher power levels, or a separate offset can be placed in the calibration routine that adds offsets for changes in temperature.

Figure 57 shows a two-point calibration like Figure 55 but the calibration points were changed from -40 dBm and -21 dBm to -39 dBm and -11 dBm. This demonstrates how calibration points can be adjusted to increase dynamic range at the expense of linearity. The higher power calibration point was moved to a point where the AD8363 is not as linear. At 25°C , there is an error of 0 dB at the calibration points. Note that the range over which the AD8363 maintains an error of $<\pm 0.5$ dB is extended to $+53$ dB at 25°C . The disadvantage of this approach is that linearity suffers and the linearity at -25 dBm degrades by about 0.2 dB and the error at $+3$ dBm increases by about 0.7 dB.

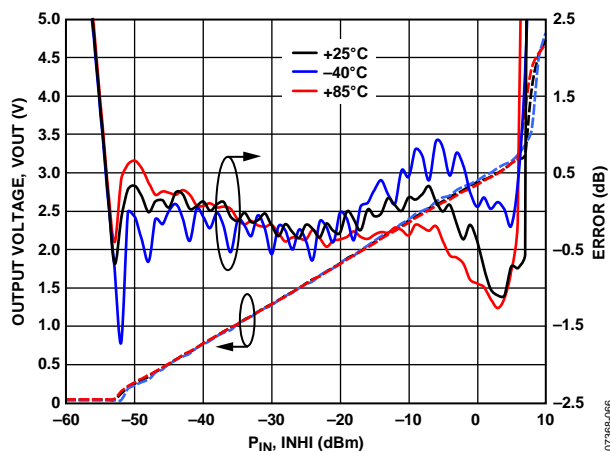


Figure 57. 2.14 GHz Transfer Function with Change in Two-Point Calibration Points

ALTERING THE SLOPE

None of the changes to operating conditions discussed so far effect the AD8363 logarithmic slope. The slope of the AD8363 can be easily increased or decreased. To reduce the slope, add a voltage divider on the output, V_{OUT} . To increase the slope, control the fraction of V_{OUT} that is fed back to the setpoint interface at the V_{SET} pin. When the full signal from V_{OUT} is applied to V_{SET} , the slope assumes its nominal value of 52 mV/dB. It can be increased by including a voltage divider between these pins, as shown in Figure 58.

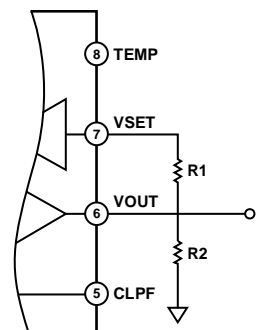


Figure 58. Altering the Slope

Use moderately low resistance values to minimize the scaling errors from the approximately $72\text{ k}\Omega$ input resistance at the V_{SET} pin. Note that this resistor string also loads the output, and eventually, it reduces the load driving capabilities, if very low values are used. Equation 19 can be used to calculate the resistor values.

$$R1 = R2' (S_D/52 - 1) \quad (19)$$

where:

S_D is the desired slope, expressed in mV/dB.

$R2'$ is the value of $R2$ in parallel with $72\text{ k}\Omega$.

The typical slope of the AD8363 is 52; adjust this as needed.

Figure 59 shows a comparison between the regular slope of a part and when the slope is doubled. For this example, $R1 = 1.65\text{ k}\Omega$ and $R2 = 1.69\text{ k}\Omega$ ($R2' = 1.65\text{ k}\Omega$). The initial slope was 52 mV/dB, and it increased to 104 mV/dB. The choice of 100 mV/dB scaling is useful when the output is applied to a digital voltmeter because the displayed number directly reads as a decibel quantity with only a decimal point shift.

When measuring a particular section of the input range, operating at a high slope is useful. With a slope of 104 mV/dB, a measurement range of 50 dB corresponds to a 5.2 V change in V_{OUT} , exceeding the capacity of the output stage of the AD8363, when operating on a 5 V supply. Figure 59 clearly shows this effect.

When interfacing with an ADC, use as much of the input dynamic range as possible to maximize the resolution. It is also important that the V_{OUT} voltage of the AD8363 does not exceed the range accepted by the input of the ADC for the power levels of interest. This must take into account the part-to-part variation of the AD8363 and its variation over temperature. This is especially important when the slope is increased. The V_{OUT} distribution is well characterized at major frequencies bands in the Typical Performance Characteristics section. Most of the V_{OUT} variation from part to part and over temperature is due to an intercept shift; therefore, increasing the slope should not increase the distribution greatly. When increasing the slope, the intercept does not change greatly. In Figure 59, the intercept changed by 0.2 dB after the slope change. Therefore, it is possible to calculate the maximum voltage for a particular power level by using the following equation:

$$New V_{MAX} = Old V_{MAX} (New Slope/Old Slope) \quad (20)$$

For example, Figure 10 shows that the maximum voltage for a -20 dBm input at 1.9 GHz is 2 V. If the slope is doubled from 52 mV/dB to 104 mV/dB, the maximum voltage at the new slope is 4 V. The REF_{IN} voltage of the ADC (the voltage that sets the maximum readable voltage in the ADC) is set to 4.16 V, assuming a 3 dB margin on its input.

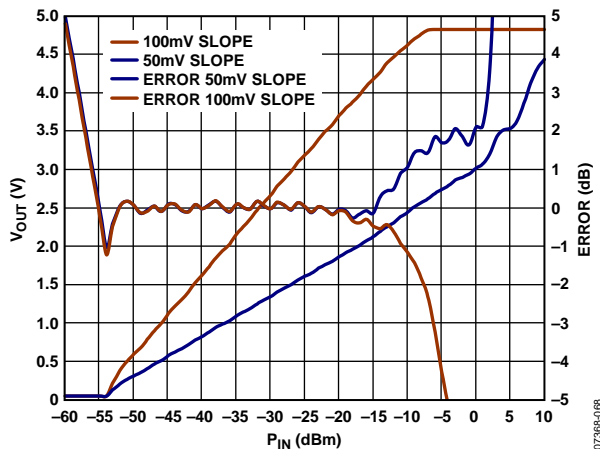


Figure 59. Slope Change from 52 mV/dB to 104 mV/dB, Frequency = 2.14 GHz

OFFSET COMPENSATION/MINIMUM C_{LPF} AND MAXIMUM C_{HPF} CAPACITANCE VALUES

An offset-nulling loop is used to address small dc offsets within the internal VGA as shown in Figure 60. The high-pass corner frequency of this loop is set to about 1 MHz using an on-chip 25 pF capacitor, which is sufficiently low for most RF applications. The high-pass corner can be lowered further by connecting a capacitor between $CHPF$ and $VPOS$.

The input offset voltage varies depending on the actual gain at which the VGA is operating and, therefore, on the input signal amplitude. When a large C_{HPF} value is used, the offset correction process can lag the more rapid changes in the gain of the VGA, which can increase the time required for the loop to fully settle for a given steady input amplitude. This can manifest itself in a jumpy, seemingly oscillatory response of the AD8363.

In measurement mode, take care in choosing C_{HPF} and C_{LPF} because there is a potential to create oscillations. In general, make the capacitance on the $CLPF$ pin as large as possible; there is no maximum on the amount of capacitance that can be added to this pin. Generally, there is no need for an external capacitor on the $CHPF$ pin; therefore, the pin can be left open. However, when trying to get a fast response time and/or when working at low frequencies, extra care in choosing the proper capacitance values for C_{HPF} and C_{LPF} is prudent. With the gain control pin ($VSET$) connected to $VOUT$, $VSET$ can slew at a rate determined by the on-chip squaring cell and C_{LPF} . When $VSET$ is changing with time, the dc offsets in the VGA also vary with time. The speed at which $VSET$ slews can create a time varying offset that falls within the high-pass corner set by C_{HPF} . Therefore, in measurement mode, take care to set C_{LPF} appropriately to reduce the slew. It is also worth noting that most of the typical performance data was derived with $C_{LPF} = 3.9$ nF and $C_{HPF} = 2.7$ nF and with a CW waveform.

The minimum appropriate C_{LPF} based on slew rate limitations is as follows

$$C_{LPF} > 20 \times 10^{-3} / FREQ_{REFIN} \quad (21)$$

where:

C_{LPF} is in farads.

$FREQ_{REFIN}$ is in hertz.

This takes into account the on-chip 25 pF capacitor, C_F , in parallel with C_{LPF} . However, because there are other internal device time delays that affect loop stability, use a minimum C_{LPF} of 390 pF.

The minimum appropriate C_{HPF} for a given high-pass pole frequency is

$$C_{HPF} = 29.2 \times 10^{-6} / FHP_{POLE} - 25 \text{ pF} \quad (22)$$

where FHP_{POLE} is in hertz.

The subtraction of 25 pF is a result of the on-chip 25 pF capacitor in parallel with the external C_{HPF} . Typically, choose C_{HPF} to give a pole (3 dB corner) at least 1 decade below the desired signal frequency. Note that the high pass corner of the offset compensation system is approximately 1 MHz without an external C_{HPF} ; therefore, adding an external capacitor lowers the corner frequency.

The following example illustrates the proper selection of the input coupling capacitors, minimum C_{LPF} , and maximum C_{HPF} when using the AD8363 in measurement mode for a 1 GHz input signal.

1. Choose the input coupling capacitors that have a 3 dB corner at least one decade below the input signal frequency. From Equation 8, $C > 10 / (2 \times \pi \times R_{FIN} \times 50) = 32 \text{ pF}$ minimum. According to this calculation, 32 pF is sufficient; however, the input coupling capacitors should be a much larger value, typically 0.1 μF . The offset compensation circuit, which is connected to C_{HPF} , should be the true determinant of the system high-pass corner frequency and not the input coupling capacitors. With 0.1 μF coupling capacitors, signals as low as 32 kHz can couple to the input, which will be well below the system high-pass frequency.
2. Choose C_{LPF} to reduce instabilities due to V_{SET} slew rate. See Equation 21, where $FRQ_{RFIN} = 1 \text{ GHz}$, and this results in $C_{LPF} > 20 \text{ pF}$. However, as previously mentioned, values below 390 pF are not recommended. For this reason, a 470 pF capacitor was chosen. In addition, if fast response times are not required, an even larger C_{LPF} value than given here should be chosen.
3. Choose C_{HPF} to set a 3 dB corner to the offset compensation system. See Equation 22, where $F_{HP_{POLE}}$ is in this case 100 MHz, one decade below the desired signal. This results in a negative number and, obviously, a negative value is not practical. Because the high-pass corner frequency is already 1 MHz, this result simply illustrates that the appropriate solution is to use no external C_{HPF} capacitor.

It can also be noted that per Equation 9

$$Freq_{LP} \approx 1.83 \times I_{TGT} / (C_{LPF})$$

A C_{LPF} of 470 pF results in a small signal low-pass corner frequency of approximately 144 kHz. This reflects the bandwidth of the measurement system, and how fast the user can expect changes on the output. It does not imply any limitations on the input RF carrier frequency.

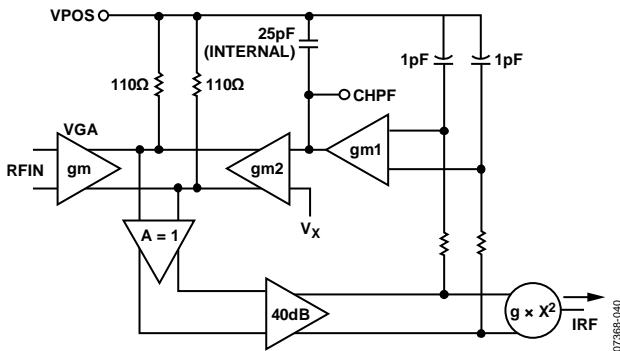


Figure 60. Offset Compensation Circuit

CHOOSING A VALUE FOR C_{LPF}

The Small Signal Loop Response section and the Offset Compensation/Minimum C_{LPF} and Maximum C_{HPF} Capacitance Values section discussed how to choose the minimum value capacitance for C_{LPF} based on a minimum capacitance of 390 pF, slew rate limitation, and frequency of operation. Using the minimum value for C_{LPF} allows the quickest response time for pulsed type waveforms (such as WiMAX) but also allows the most residual ripple on the output caused by the pseudorandom modulation waveform. There is not a maximum for the capacitance that can be applied to the C_{LPF} pin, and in most situations, a large enough capacitor can be added to remove the residual ripple caused by the modulation and yet allow a fast enough response to changes in input power.

Figure 61 shows how residual ripple, rise time, and fall time vary with filter capacitance when the AD8363 is driven by a single carrier CDMA2000 9CH SR1 signal at 2.14 GHz. The rise time and fall time is based on a signal that is pulsed between no signal and 10 dBm but is faster if the input power change is less.

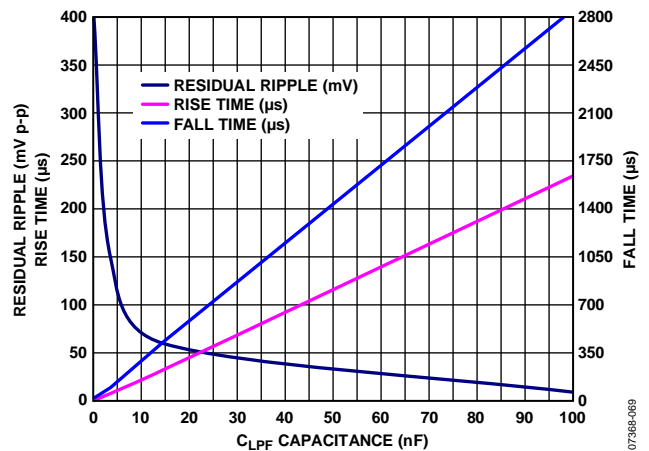


Figure 61. Residual Ripple, Rise Time, and Fall Time vs. C_{LPF} Capacitance, Single Carrier CDMA2000 9CH SR1 Signal at 2.14 GHz with 10 dBm Pulse

AD8363

Table 5 shows the recommended values of C_{LPF} for popular modulation schemes. For nonpulsed waveforms, increase C_{LPF} until the residual output noise falls below 50 mV (± 0.5 dB). In each case, the capacitor can be increased to further reduce the noise. A 10% to 90% step response to an input step is also listed. Where the increased response time is unacceptably high, reduce C_{LPF} , which increases the noise on the output. Due to the random nature of the output ripple, if it is sampled by an ADC, averaging in the digital domain further reduces the residual noise.

Table 5 gives C_{LPF} values to minimize noise while trying to keep a reasonable response time. For nonpulsed type waveforms, averaging is not required on the output. For pulsed waveforms, the smaller the noise, the less averaging is needed on the output.

System specifications determine the necessary rise time and fall time. For example, the suggested C_{LPF} value for WiMAX assumes that it is not necessary to measure the power in the preamble. Figure 62 shows how the rise time cuts off the preamble. Note that the power in the preamble can be easily measured; however, the C_{LPF} value would have to be reduced slightly, and the noise in the main signal would increase.

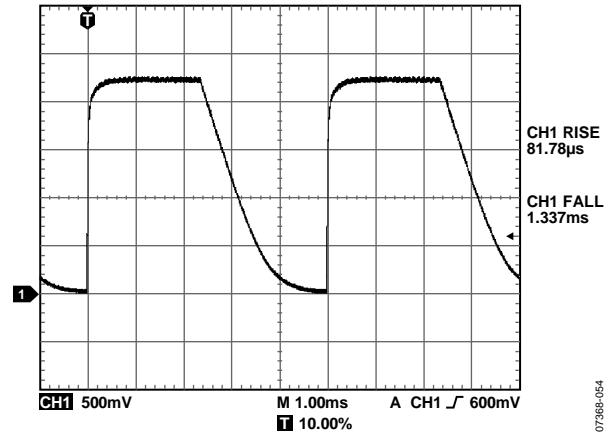


Figure 62. AD8363 Output to a WiMAX 802.16, 64 QAM, 256 Subcarriers, 10 MHz Bandwidth Signal with $C_{LPF} = 0.027 \mu\text{F}$

As shown in Figure 61, the fall time for the AD8363 increases faster than the rise time with an increase in C_{LPF} capacitance. Some pulse-type modulation standards require a fast fall time as well as a fast rise time, and in all cases, less output ripple is desired. Placing an RC filter on the output reduces the ripple, according to the frequency content of the ripple and the filter's poles and zeros. Using an RC output filter also changes the rise and fall time vs. the output ripple response as compared to increasing the C_{LPF} capacitance.

Table 5. Recommended C_{LPF} Values for Various Modulation Schemes

Modulation/Standard	Crest Factor (dB)	C_{LPF}	Residual Ripple (mV p-p)	Response Time (Rise/Fall) 10% to 90%
W-CDMA, 1Carrier, TM1-64	12	0.1 μF	15	236 μs /2.9 ms
W-CDMA, 1Carrier, TM1-64 (EVDO)	12	3900 pF	150	8.5 μs /100 μs
W-CDMA 4Carrier, TM1-64	11	0.1 μF	8	240 μs /2.99 ms
CDMA2000, 1Carrier, 9CH	9.1	0.1 μF	10	210 μs /3.1 ms
CDMA2000, 3Carrier, 9CH	11	0.1 μF	13	215 μs /3.14 ms
WiMAX 802.16, 64 QAM, 256 Subcarriers, 10 MHz Bandwidth	14	0.027 μF	10	83 μs /1.35 ms
6C TD-SCDMA	14	0.01 μF	69	24 μs /207 μs
1C TD-SCDMA	11.4	0.01 μF	75	24 μs /198 μs

Figure 63 shows the response for a 2.14 GHz pulsed signal, with $C_{LPF} = 3900$ pF. The residual ripple from a single carrier CDMA2000 9CH SR1 signal is 150 mV p-p. (The ripple is not shown in Figure 63. The ripple was measured separately.) Figure 64 shows the response for a 2.14 GHz pulse signal with a C_{LPF} of 390 pF and an output filter that consists of a series 75 Ω resistor (closest to the output) followed by a 0.15 μ F capacitor to ground. The residual ripple for this configuration is also 150 mV p-p. Note that the rise time is faster and the fall time is slower when the larger C_{LPF} is used to obtain a 150 mV p-p ripple.

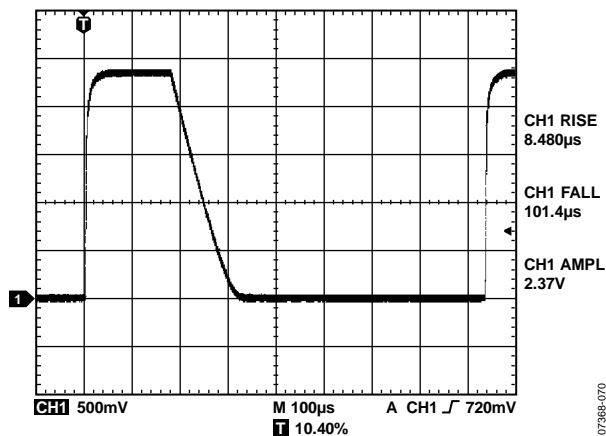


Figure 63. Pulse Response with $C_{LPF} = 3900$ pF Resulting in a 150 mV p-p Ripple for a Single Carrier CDMA2000 9CH SR1 Signal at 2.14 GHz

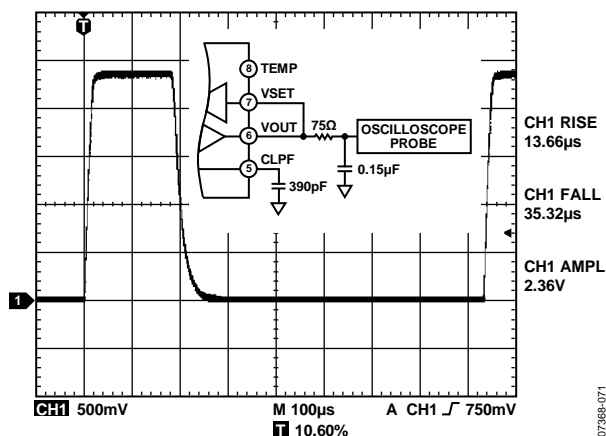


Figure 64. Pulse Response with $C_{LPF} = 390$ pF and Series 75 Ω Resistor Followed by a 0.15 μ F Capacitor to Ground, Resulting in a 150 mV p-p Ripple for a Single Carrier CDMA2000 9CH SR1 Signal at 2.14 GHz

RF PULSE RESPONSE

The response of the AD8363 to pulsed RF waveforms is affected by V_{TGT} . Referring to Figure 33 and Figure 34, there is a period of inactivity between the start of the RF waveform and the time at which V_{OUT} begins to show a reaction. This happens as a result of the implementation of the balancing of the squarer currents within the AD8363. This delay can be reduced by decreasing V_{TGT} ; however, as previously noted in the V_{TGT} Interface section, this has implications on the sensitivity, intercept, and dynamic range. While the delay is reduced, reducing V_{TGT} increases the rise and fall time of V_{OUT} .

CONTROLLER MODE BASIC CONNECTIONS

In addition to being a measurement device, the AD8363 can also be configured to control rms signal levels, as shown in Figure 65.

The RF input to the device is configured as it was in measurement mode and either input can be used. A directional coupler taps off some of the power being generated by the VGA. If loss in the main signal path is not a concern, and there are no issues with reflected energy from the next stage in the signal chain, a power splitter can be used instead of a directional coupler. Some additional attenuation may be required to set the maximum input signal at the AD8363 to be equal to the recommended maximum input level for optimum linearity and temperature stability at the frequency of operation.

The VSET and VOUT pins are no longer shorted together. VOUT now provides a bias or gain control voltage to the VGA. The gain control sense of the VGA must be negative and monotonic, that is, increasing voltage tends to decrease gain. However, the gain control transfer function of the device does not need to be well controlled or particularly linear. If the gain control sense of the VGA is positive, an inverting op amp circuit with a dc offset shift can be used between the AD8363 and the VGA to keep the gain control voltage in the 0.03 V to 4.8 V range.

VSET becomes the set-point input to the system. This can be driven by a DAC, as shown in Figure 65, if the output power is expected to vary, or it can simply be driven by a stable reference voltage, if constant output power is required. This DAC should have an output swing that covers the 0.15 V to 3.5 V range. The AD7391 and AD7393 serial input and parallel input 10-bit DACs provide adequate resolution (4 mV/bit) and an adjustable output swing over 4.5 V.

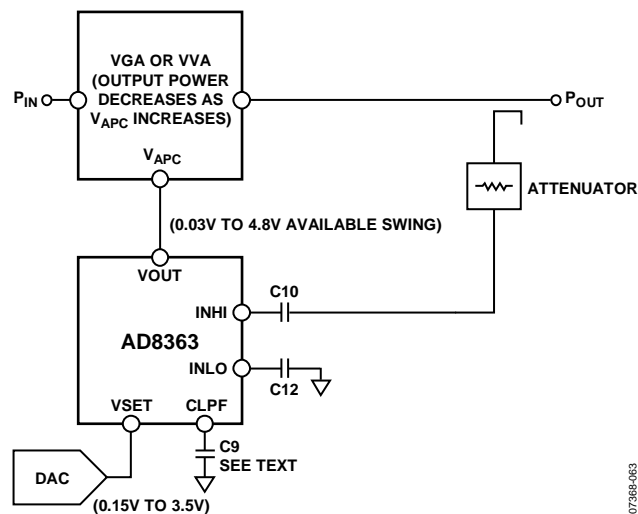


Figure 65. Controller Mode Operation for Automatic Power Control

AD8363

When V_{SET} is set to a particular value, the AD8363 compares this value to the equivalent input power present at the RF input. If these two values do not match, V_{OUT} increases or decreases in an effort to balance the system. The dominant pole of the error amplifier/integrator circuit that drives V_{OUT} is set by the capacitance on the CLPF pin; some experimentation may be necessary to choose the right value for this capacitor.

In general, C_{LPF} should be chosen to provide stable loop operation for the complete output power control range. If the slope (in dB/V) of the gain control transfer function of the VGA is not constant, C_{LPF} must be chosen to guarantee a stable loop when the gain control slope is at its maximum. In addition, C_{LPF} must provide adequate averaging to the internal low range squaring detector so that the rms computation is valid. Larger values of C_{LPF} tend to make the loop less responsive.

The relationship between V_{SET} and the RF input follows the measurement mode behavior of the device. For example, Figure 6 shows the measurement mode transfer function at 900 MHz and that an input power of -10 dBm yields an output voltage of approximately 2.5 V. Therefore, in controller mode, if V_{SET} is 2.5 V, the AD8363 output would go to whatever voltage is necessary to set the AD8363 input power to -10 dBm.

CONSTANT OUTPUT POWER OPERATION

In controller mode, the AD8363 can be used to hold the output power of a VGA stable over a broad temperature/input power range. This is useful in topologies where a transmit card is driving an HPA, or when connecting any two power sensitive modules together. Figure 66 shows a schematic of a circuit setup that holds the output power to approximately -26 dBm at 2.14 GHz, when the input power is varied over a 40 dB dynamic range. Figure 67 shows the results. A portion of the output power is coupled off using a 10 dB coupler, and it is then fed into the AD8363. V_{SET} is fixed at 0.95 V, which forces the AD8363 output voltage to control the ADL5330 so that the input to the AD8363 is approximately -36 dBm. If the AD8363 was in measurement mode and a -36 dBm input power is applied, the output voltage would be 0.95 V. A general-purpose, rail-to-rail op amp (AD8062) is used to invert the slope of the AD8363 so that the gain of the ADL5330 decreases as the AD8363 control voltage increases. The output power is controlled to a 10 dB higher power level than that seen by the AD8363 due to the coupler. The high end power is limited by the linearity of the VGA (ADL5330) with high attenuation and can be increased by using a higher linearity VGA.

The low end power is limited by the maximum gain of the VGA (ADL5330) and can be increased by using a VGA with more gain. The temperature performance is directly related to the temperature performance of the AD8363 at 2.14 GHz and -26 dBm, using $TCM1 = 0.52$ V and $TCM2 = 0.6$ V. All other temperature variations are removed by the AD8363.

For more information on controller mode, see the Controller Mode Basic Connections section.

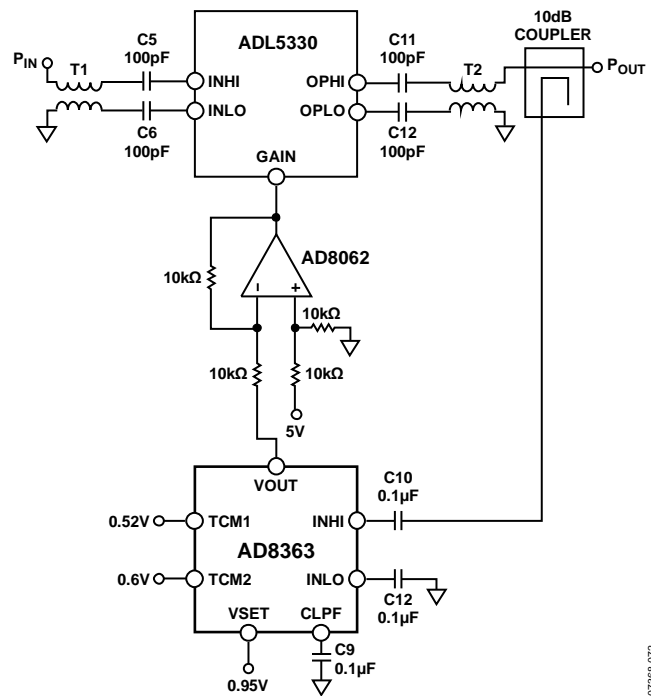


Figure 66. Constant Power Circuit

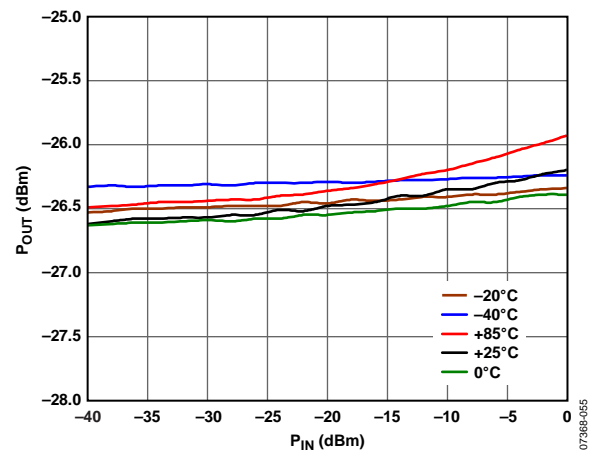


Figure 67. Performance of the Circuit Shown in Figure 66

DESCRIPTION OF RF CHARACTERIZATION

The general hardware configuration used for most of the AD8363 characterization is shown in Figure 68. The AD8363 was driven in a single-ended configuration for all characterization.

Characterization of the AD8363 employed a multisite test strategy. Several AD8363 devices mounted on circuit boards constructed with Rogers 3006 material was simultaneously inserted into a remotely-controlled thermal test chamber. A Keithley S46 RF switching network connected an Agilent E8251A signal source to the appropriate device under test. An Agilent 34980A switch matrix provided switching of dc power and metering for the test sites. A PC running Agilent VEE Pro controlled the signal source, switching, and chamber temperature.

A voltmeter measured the subsequent response to the stimulus, and the results were stored in a database for later analysis. In this way, multiple AD8363 devices were characterized over amplitude, frequency, and temperature in a minimum amount of time.

The RF stimulus amplitude was calibrated up to the connector of the circuit board that carries the AD8363. However, the calibration does not account for the slight losses due to the connector and the traces from the connector to the device under test. For this reason, there is a small absolute amplitude error (<0.5 dB) not accounted for in the characterization data.

This implies a slight error in the reported intercept; however, this is generally not important because the slope and the relative accuracy of the AD8363 are not affected.

The typical performance data was derived with $C_{LPF} = 3.9 \text{ nF}$ and $C_{HPF} = 2.7 \text{ nF}$ with a CW waveform.

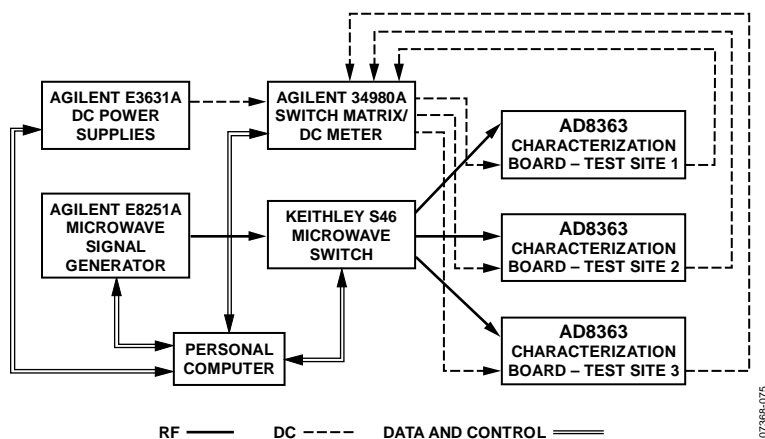


Figure 68. General RF Characterization Configuration

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AD8363

EVALUATION AND CHARACTERIZATION CIRCUIT BOARD LAYOUTS

Figure 69 to Figure 73 show the evaluation board for the AD8363.

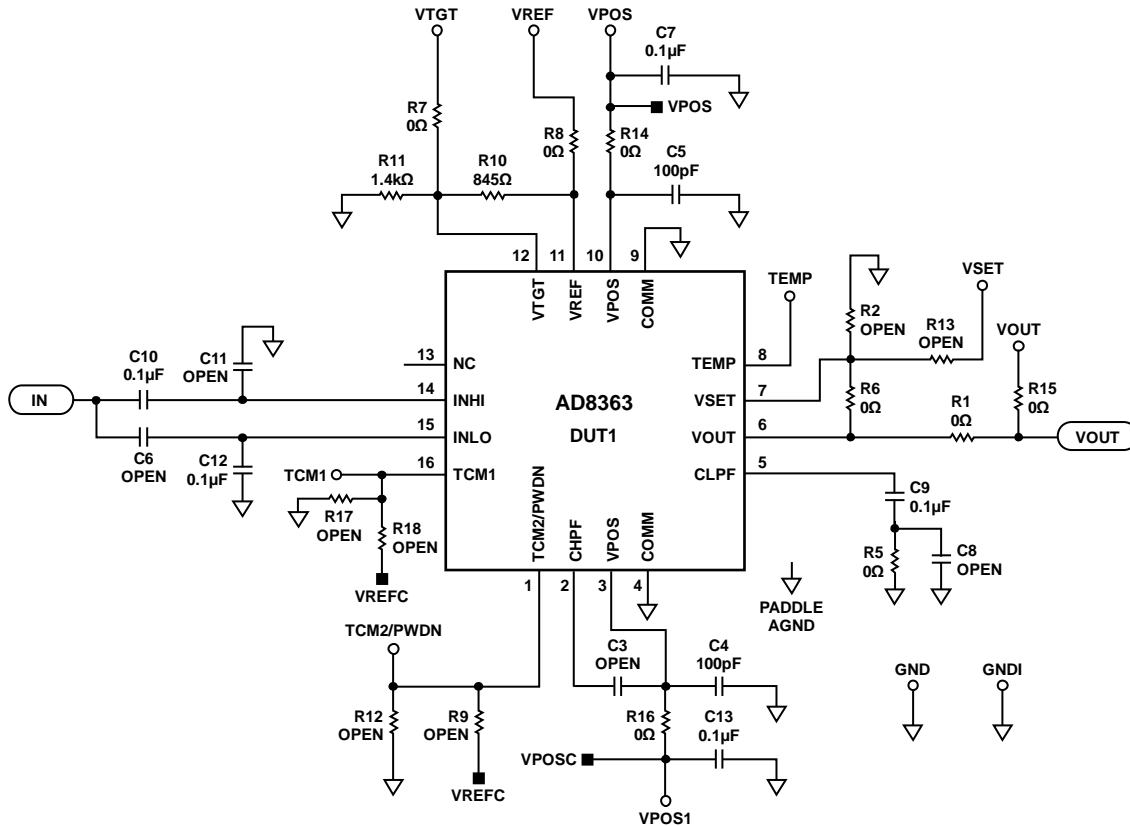


Figure 69. Evaluation Board Schematic

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Table 6. Bill of Materials

Component	Function/Notes	Default Value
C6, C10, C11, C12	Input. The AD8363 is single ended driven. At frequencies ≤ 2.6 GHz, the best dynamic range is achieved by driving Pin 14 (INHI). When driving INHI, populate C10 and C12 with an appropriate capacitor value for the frequency of operation and leave C6 and C11 open. For frequencies > 2.6 GHz, additional dynamic range can be achieved by driving Pin 15 (INLO). When driving INLO, populate C6 and C11 with an appropriate capacitor value for the frequency of operation and leave C10 and C12 open.	C6 = open, C10 = 0.1 μ F, C11 = open C12 = 0.1 μ F
R7, R8, R10, R11	VTGT. R10 and R11 are set up to provide 1.4 V to VTGT from VREF. If R10 and R11 are removed, an external voltage can be used. Alternatively, R7 and R11 can be used to form a voltage divider for an external reference.	R7 = 0 Ω , R8 = 0 Ω , R10 = 845 Ω , R11 = 1.4 k Ω
C4, C5, C7, C13, R14, R16	Power Supply Decoupling. The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8363, a 0 Ω series resistor, and a 0.1 μ F capacitor placed close to the power supply input pin. The 0 Ω resistor can be replaced with a larger resistor to add more filtering; however, it is at the expense of a voltage drop.	C4 = 100 pF, C5 = 100 pF, C7 = 0.1 μ F, C13 = 0.1 μ F, R14 = 0 Ω , R16 = 0 Ω

Component	Function/Notes	Default Value
R1, R2, R6, R13, R15	<p>Output Interface (Default Configuration) in Measurement Mode. In this mode, a portion of the output voltage is fed back to the VSET pin via R6. Using the voltage divider created by R2 and R6, the magnitude of the slope at VOUT is increased by reducing the portion of VOUT that is fed back to VSET. If a fast responding output is expected, the 0 Ω resistor (R15) can be removed to reduce parasitics on the output.</p> <p>Output Interface in Controller Mode. In this mode, R6 must be open and R13 must have a 0 Ω resistor. In controller mode, the AD8363 can control the gain of an external component. A setpoint voltage is applied to the VSET pin, the value of which corresponds to the desired RF input signal level applied to the AD8363. If a fast responding output is expected, the 0 Ω resistor (R15) can be removed to reduce parasitics on the output.</p>	R1 = 0 Ω , R2 = open, R6 = 0 Ω , R13 = open, R15 = 0 Ω
C8, C9, R5	Low-Pass Filter Capacitors, C_{LPF} . The low-pass filter capacitors reduce the noise on the output and affect the pulse response time of the AD8363. This capacitor should be as large as possible. The smallest C_{LPF} capacitance should be 390 pF. R5, when set to a value other than 0 Ω , is used in conjunction with C8 and C9 to modify the loop transfer function and change the loop dynamics in controller mode.	C8 = open, C9 = 0.1 μ F, R5 = 0 Ω
C3	C_{HPF} Capacitor. The C_{HPF} capacitor introduces a high-pass filter affect into the AD8363 transfer function and can also affect the response time. The C_{HPF} capacitor should be as small as possible and connect to VPOS when used. No capacitor is needed for input frequencies greater than 10 MHz.	C3 = open
R9, R12	TCM2/PWDN. The TCM2/PWDN pin controls the amount of nonlinear intercept temperature compensation and/or shuts down the device. The evaluation board is configured to control this from a test loop, but VREF can also be used by the voltage divider created by R9 and R12.	R9 = open, R12 = open
R17, R18	TCM1. TCM1 controls the temperature compensation (5 k Ω impedance). The evaluation board is configured to control this from a test loop, but VREF can also be used by the voltage divider created by R17 and R18. Due to the relatively low impedance of the TCM1 pin and the limited current of the VREF pin, care should be taken when choosing the R17 and R18 values.	R17 = open, R18 = open
Paddle	Connect the paddle to both a thermal and electrical ground.	

ASSEMBLY DRAWINGS

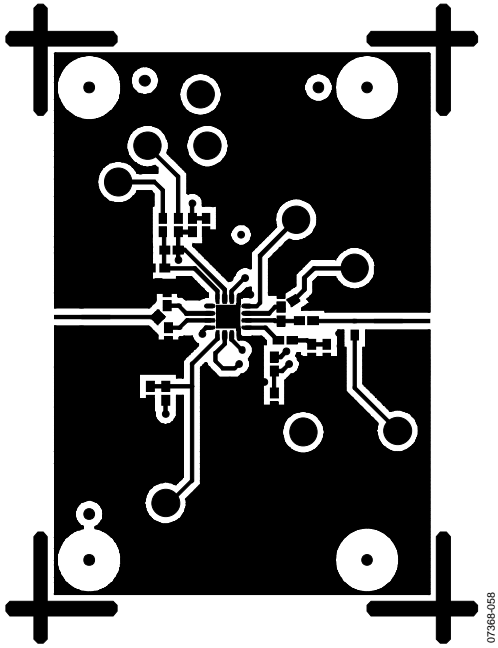


Figure 70. Evaluation Board Layout, Top Side

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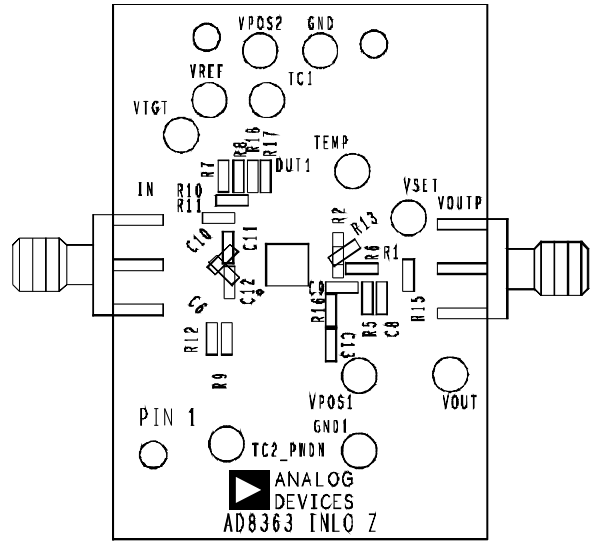


Figure 72. Evaluation Board Assembly, Top Side

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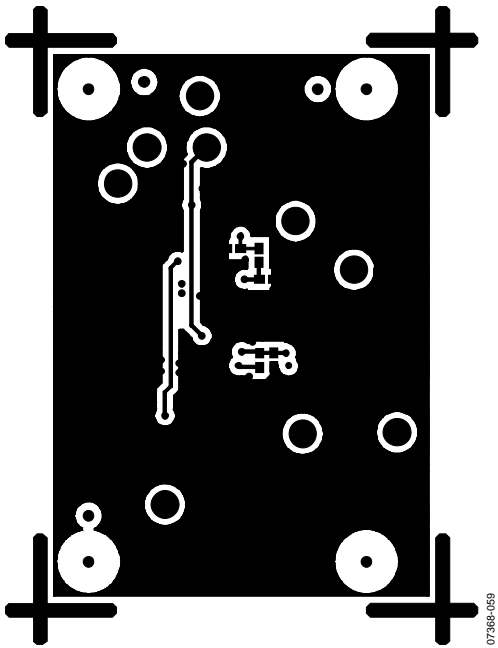


Figure 71. Evaluation Board Layout, Bottom Side

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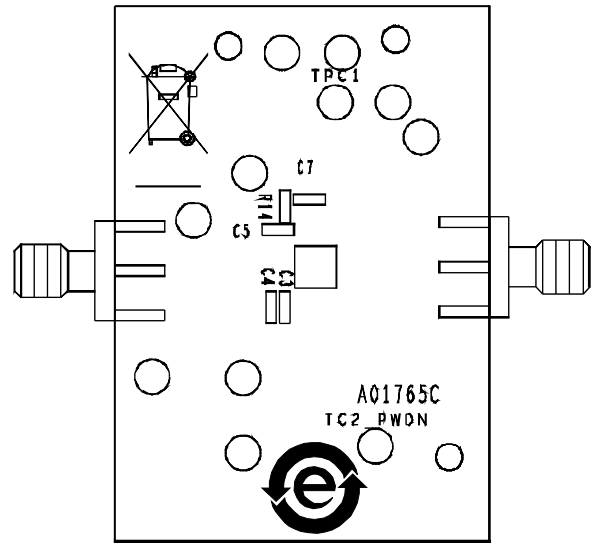
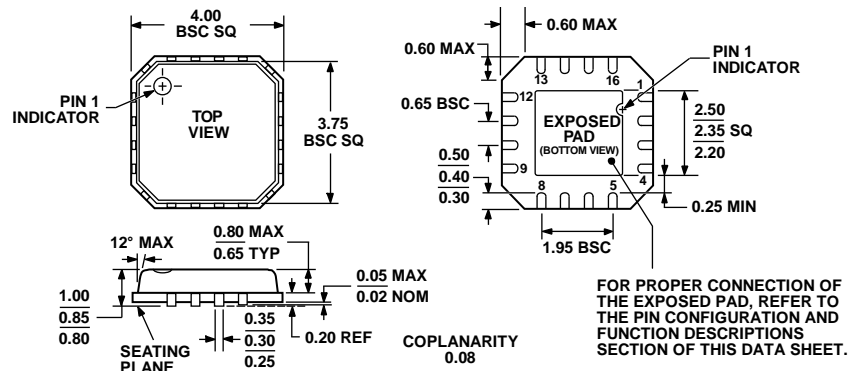


Figure 73. Evaluation Board Assembly, Bottom Side

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OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 74. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 4 mm × 4mm Body, Very Thin Quad
 (CP-16-10)
 Dimensions shown in millimeters

082008-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8363ACPZ-R7 ¹	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	1,500
AD8363ACPZ-WP ¹	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-10	64
AD8363-EVALZ ¹		Evaluation Board		

¹ Z = RoHS Compliant Part.

AD8363

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